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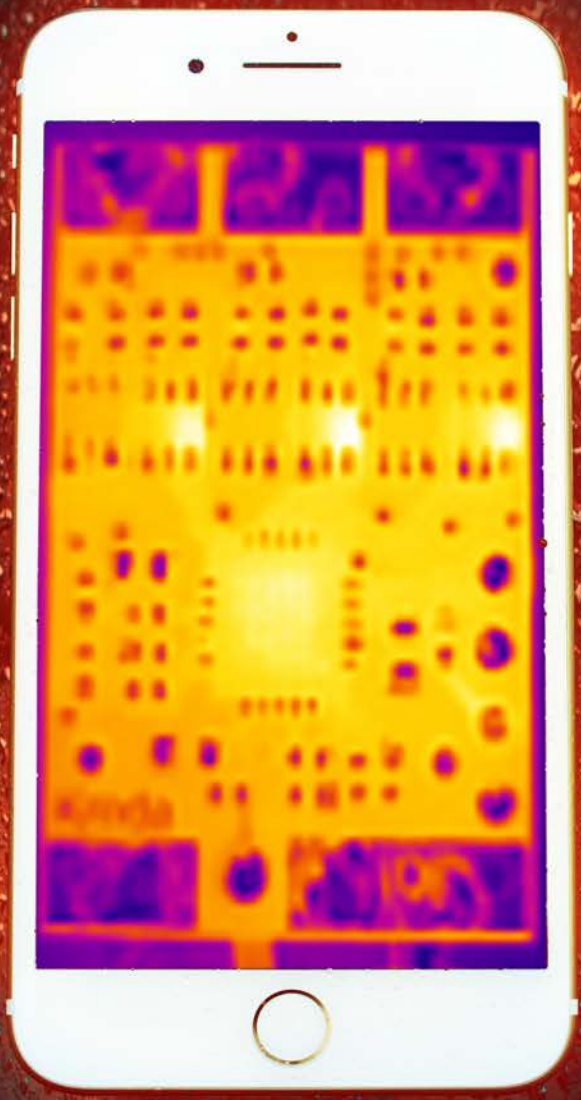
A Figure of Merit for Smart Phone Thermal Management



Solder Joint Lifetime of Rapidly Cycled LED Components

Keeping Moore's Law Alive

Calculations for Thermal Interface Materials

Historical Suggestions for Thermal Management of Electronics

SEMI-THERM 33 2017 Exhibits Highlights

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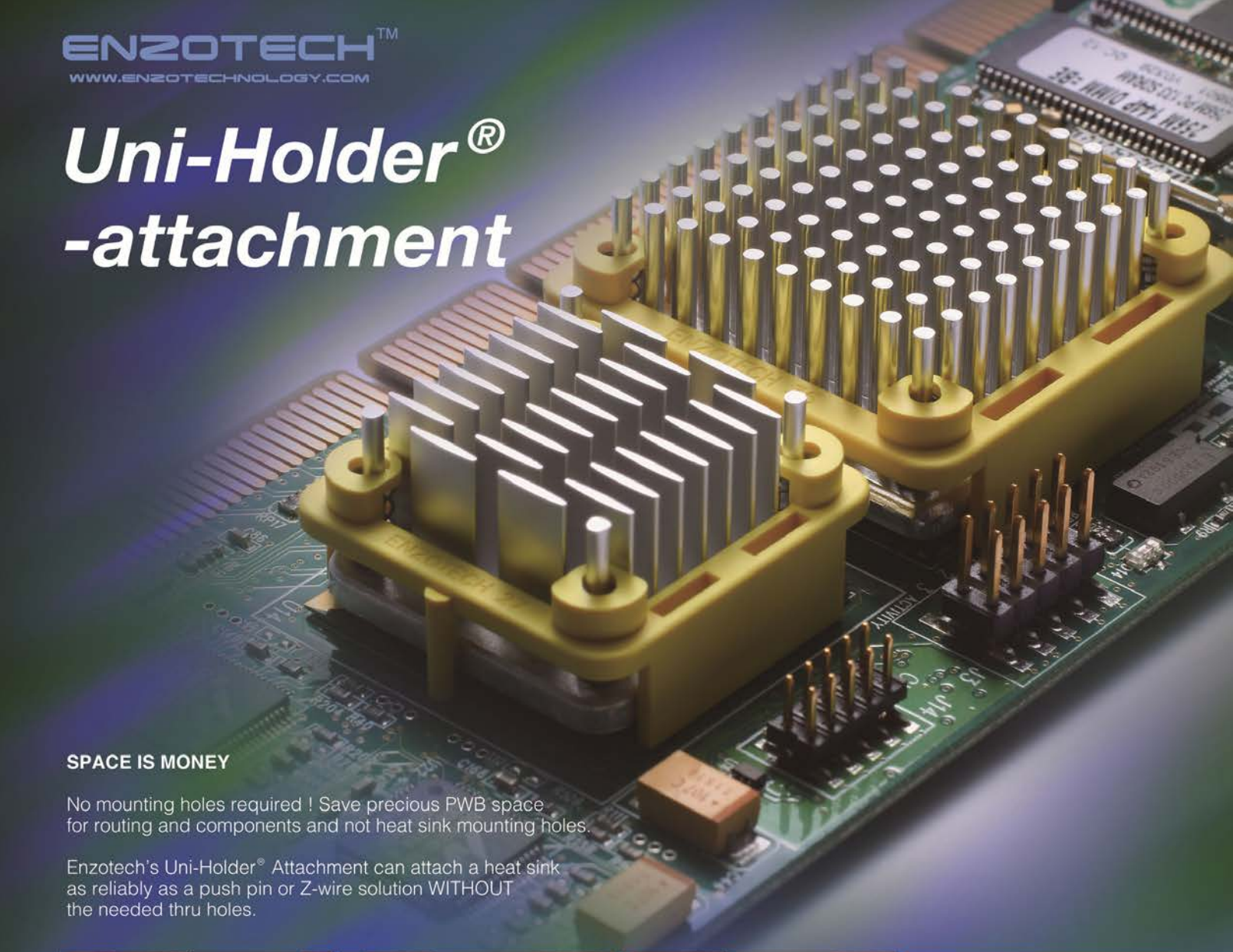
Uni-Holder® -attachment



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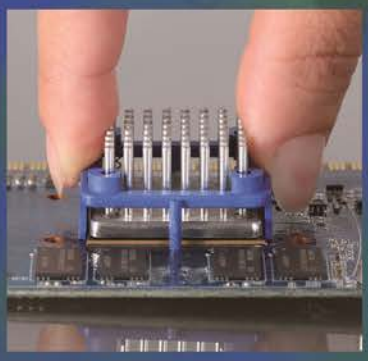
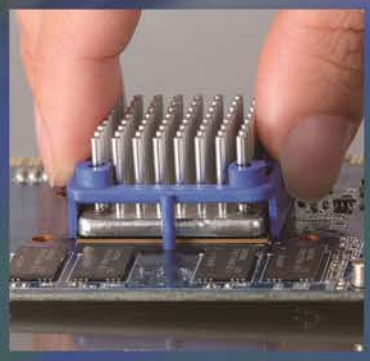
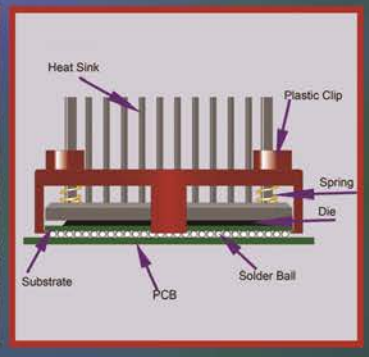


Step 2:
Press down the other side of Uni-Holder® to snap it on BGA clip.



Step 3:
Installation completed. Snap on . Stay on .



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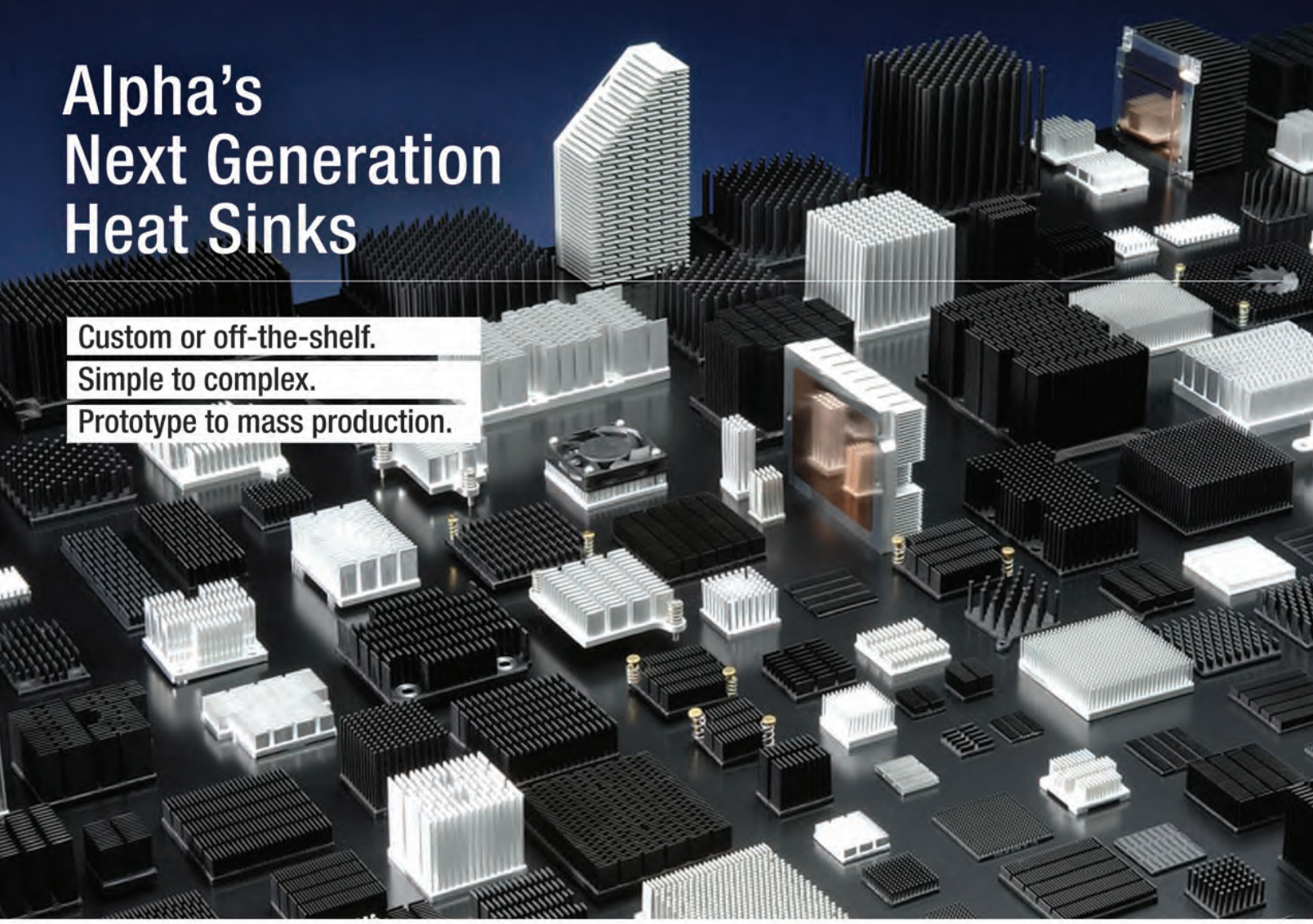

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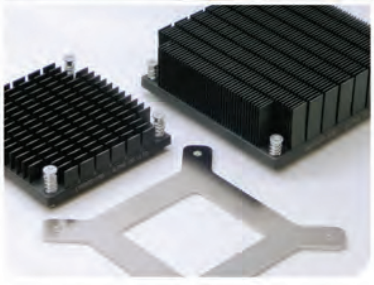

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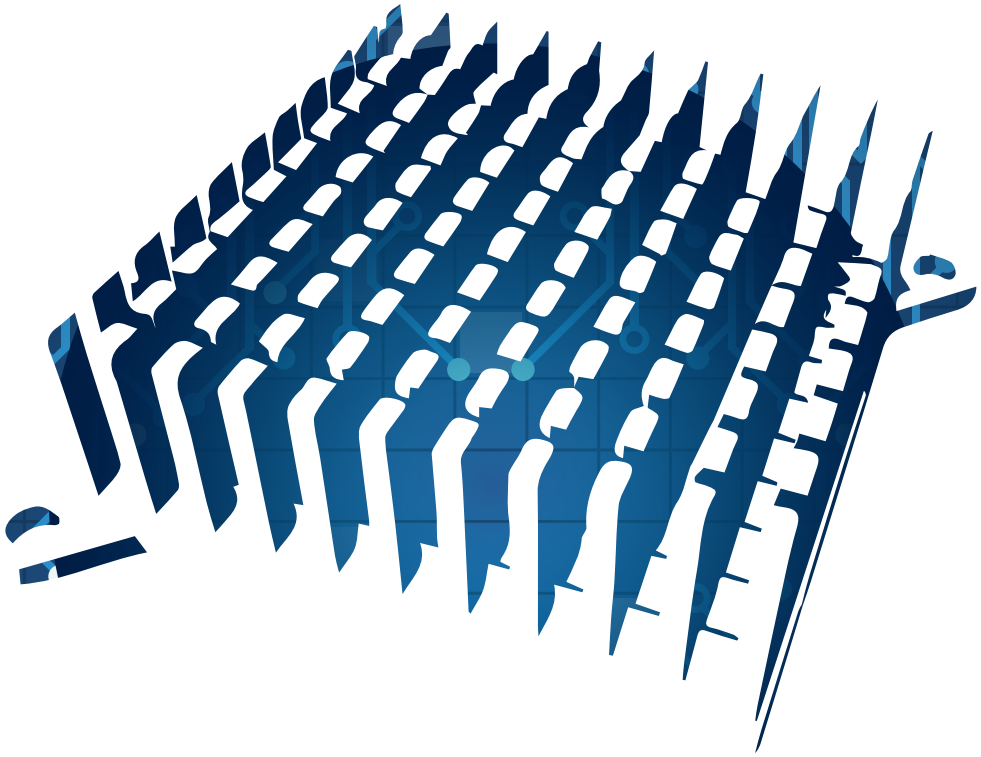

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CONTENTS

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2 EDITORIAL
MP Divakar, PHD

4 COOLING EVENTS
News of Upcoming Thermal Management Events

6 CALCULATION CORNER
Calculations for Thermal Interface Materials
Bruce Guenin

8 THERMAL FACTS & FAIRY TALES
Historical Suggestions for Thermal Management of Electronics
Jim Wilson

12 FEATURE ARTICLE
Solder Joint Lifetime of Rapidly Cycled LED Components
Ir. G. A. (Wendy) Luiten

16 FEATURE ARTICLE
A Figure of Merit for Smart Phone Thermal Management
Victor Chiriac, Steve Molloy, Jon Anderson, Ken Goodson

22 FEATURE ARTICLE
Keeping Moore's Law Alive
Peter E. Raad

31 SEMI-THERM 2017
SEMI-THERM 33 2017 Exhibits Highlights
MP Divakar, PHD

40 INDEX OF ADVERTISERS

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ITEM MEDIA

EDITORIAL

MP Divakar, PHD
Managing Editor

Over the last eight months or so I have had the opportunity to author and edit many blogs on the Electronics Cooling website. As a thermal management and electronics packaging professional, I jumped at the opportunity to work on many diverse topics of thermal management and write about them as electronics continues to pervade all walks of our lives. These months of renewed enthusiasm for thermal management have given me a quite a bit of appreciation for it as a vast, multidisciplinary, complex and intriguing yet fun-filled subject to work on. In that journey I have made many new acquaintances and forged many new professional relationships instilling a drive in me to continue to contribute to the maximum extent possible.

Electronics thermal management has come to the forefront of product design more than ever before and plays the most essential role in the product design process. More often than not, it is the first task that is performed to evaluate a concept's feasibility. Thermal management tasks these days are increasingly complex requiring much more detailed studies at the concept's feasibility stage itself. Resources and design aids such as those provided by Electronics Cooling magazine and our website continue to aid and benefit thermal management professionals to a great extent. As many readers of Electronics Cooling are familiar with, ITEM Media has been publishing the print editions of Electronics Cooling magazine for many years now and is pleased to continue that tradition for a foreseeable future.

At ITEM Media, we have been closely tracking the emerging and continuing trends in electronics product segments and their impact on thermal management. Our coverage of electronics thermal management technologies now spans across multiple disciplines –from physical sciences to biosciences and medical. For the print version, we prioritized the following as major tracks to address in the remaining print editions for the year 2017:

- Consumer Electronics & IoT
- Automotive Focus
- Military, Aerospace & Industrial Focus

This edition of Electronics Cooling magazine will feature some of the best articles from previously published editions and blogs. Our editorial board is actively working on sourcing articles for the above categories and we expect to feature them in the next release scheduled for June 2017. We are also actively seeking additions to the editorial board –please contact me if you are interested to serve.

In addition the print editions, we are also actively working on releasing miniguides that will benefit our readers working in specific segments of electronics thermal management. We hope you will make use of the debut editions of miniguides and provide us your feedback.

Lastly, your input is very important to us. Please email your comments and suggestions on this print edition, our upcoming Thermal Live! and blogs on our website to mp@electronics-cooling.com.

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COOLING EVENTS

News of Upcoming Thermal Management Events

2017 RF AND MICROWAVE PACKAGING (RAMP) CONFERENCE

April 26 (Wednesday) - 27 (Thursday)
Espace Saint-Martin / Paris, France
The objective of the RF and Microwave Packaging Workshop is to provide a unique forum that brings together scientists, engineers, manufacturing, academia, and business people from around the world who work in the area of RF and Microwave packaging technologies. This workshop enables discussion and presentation of the latest RF and Microwave technology. To help bring together the international community, this workshop is being co-sponsored by IMAPS-France and will be the continuation of a series of joint workshops on RF and Microwave packaging between IMAPS and IMAPS-France and UK Chapters.
http://www.imaps.org/rf/

THERMAL DESIGN & COOLING OF ELECTRONICS WORKSHOP

May 1 (Monday) - 3 (Wednesday)
Eindhoven, the Netherlands
Experienced lecturers Wendy Luiten (winner of the Prestigious Harvey Rosten Award 2014) and Clemens Lasance (SEMI-THERM THERMI Award winner in 2001) teach the participants how to solve the thermal problems they encounter during all levels of the product creation process. They discuss the why, what and how of thermal management.

The course is a balanced mixture between theory and practice. A real-life case obtained from the participants themselves and prepared by the lecturers is used to demonstrate the application of the course principles.

Because early knowledge of thermally related problems is imperative to prevent expensive redesigns and a delayed market introduction, thermal design should be part of the product design process from the early start.
http://www.hightechinstitute.nl/en/training/electronics/thermal_design_and_cooling_of_electronics_workshop/

VTMS 13: VEHICLE THERMAL MANAGEMENT SYSTEMS

May 17 (Wednesday) - 18 (Thursday)
London, UK
VTMS 13: dedicated to discussing the latest international developments in Vehicle Thermal Management Systems In order to reduce emissions and make all vehicles more efficient, VTMS 13 will showcase the latest research and technological advances in heat transfer, energy management, thermal comfort and the efficient integration and control of all thermal systems within the vehicle.

The programme will feature plenary sessions, breakout technical sessions, panel discussions, and a dedicated exhibition to bring you the latest product offerings from around the world, along with a great opportunity to network with the leaders in industry.
http://events.imeche.org/ViewEvent?code=CON6389

7TH INTERNATIONAL SYMPOSIUM ON ADVANCES IN COMPUTATIONAL HEAT TRANSFER (CHT-17)

May 28 (Sunday) - June 2 (Friday)
Centro Congressi Federico II / Napoli, Italy
The objective of the symposium is to provide a forum for the exchange of ideas, methods and results in computational heat transfer (CHT). Papers on all aspects of CHT – both fundamental and applied – will be welcome.
http://www.ichmt.org/site/4/cht-17

ITHERM 2017

May 30 (Tuesday) - June 2 (Friday)
Walt Disney World Swan & Dolphin Hotel / Lake Buena Vista, Florida
Sponsored by the IEEE's CPMT Society, ITherm 2017 is an international conference for scientific and engineering exploration of thermal, thermomechanical and emerging technology issues associated with electronic devices, packages and systems. ITherm 2017 will be held along with the 66th Electronic Components and Technology Conference, a premier electronics packaging conference. Dual-registration for ITHERM and ECTC is offered at a substantial discount. In addition to Oral and poster presentations and vendor exhibits, ITherm 2017 includes panel discussions, keynote lectures by prominent speakers, a "Cutting Edge Vendors" session, a Workshop on the Industrial Internet, and professional short courses.
http://ieee-itherm.net/itherm/conference/home

AIAA THERMOPHYSICS CONFERENCE

June 5 (Monday) - 9 (Friday)
Sheraton Denver Downtown Hotel / Denver, Colorado
The Thermophysics Conference covers all aspects of thermal science and engineering related to aerospace applications. Topics range from basic research and development to applied and advanced technology, including novel experimental and computational observations, interdisciplinary papers that bridge theoretical and experimental approaches, and papers that provide innovative concepts and analyses.
http://www.aiaa-aviation.org/Thermophysics/?_ga=1.111643655.2048506410.1460490790

DESIGN AUTOMATION CONFERENCE (DAC) 2017

June 18 (Sunday) - 22 (Thursday)
Austin Convention Center / Austin, Texas
The Design Automation Conference (DAC) is recognized as the premier conference for design and automation of electronic systems. DAC offers outstanding training, education, exhibits and superb networking opportunities for designers, researchers, tool developers and vendors.
https://dac.com/content/travel-stay

Calculations for Thermal Interface Materials

Bruce Guenin
Principal Hardware Engineer, Oracle Corporation, San Diego, CA.
Editor, Electronics Cooling

It's no news to any of the readers of this publication that the increased power dissipation of integrated circuits has led to continuous refinement of package designs and component materials. This trend has increased the importance of thermal interface materials (TIMs) as a key factor in determining the thermal performance of packages intended for high-power applications. This increased importance of TIMs necessitates the use of more precise methods for determining their impact on the package thermal resistance.

PHYSICAL PICTURE

Figure 1 illustrates a typical method of packaging a high-power IC chip. In this example, the device is a flip chip with a solder bump array providing the electrical interconnection to the package substrate. The heat-generating circuitry is on the lower surface of the chip. The heat is routed out of the back of the chip – first to the package lid and then to a heat sink mounted to the top of the package. In this example, there are two TIMs: 1) joining the chip to the lid, and 2) joining the lid to the heatsink.

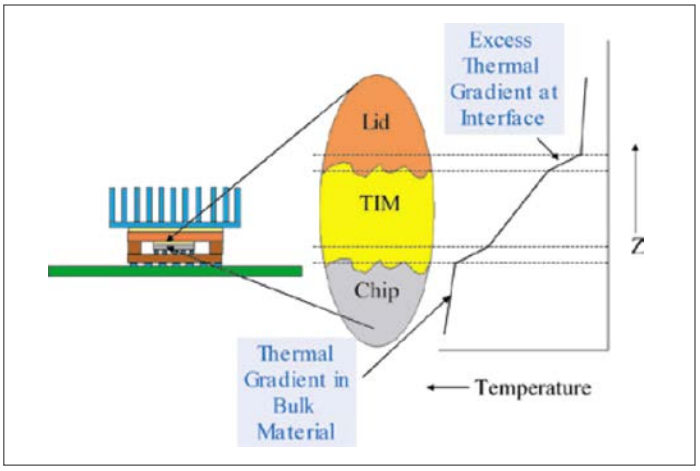


Figure 1. TIM application. Effect of bulk and interfacial thermal properties of TIM on thermal performance.

TIMs may be either low modulus materials, such as greases, gels, or phase-change materials, or higher modulus adhesives. A key function of a TIM is to provide efficient, stable, and uniform thermal coupling between two surfaces in spite of any warpage or surface roughness.

The inset in *Figure 1* illustrates the microscopically rough nature of surfaces on typical packaging components. TIMs are designed to conform to the contours of the surfaces, which contact them. However, with the materials in commercial use today, there will always be an excess thermal resistance within the interface region. This results from factors such as incomplete wetting of the surface by the TIM or the exclusion of the particulate filler materials from the interfacial region.

The graph in *Figure 1* illustrates the thermal gradients both within the bulk material and at the interface, assuming a 1-D heat flow situation. The temperature within the bulk materials decreases linearly with increased distance from the heat source. The gradient is simply related to the heat flux and the bulk thermal conductivity of each of the materials. However, in the interface regions bounding the TIM, there is an abrupt change in temperature. This excess thermal gradient at the interface depends upon the surface chemistry of materials adjoining the TIM and the method of application of the TIM, among other factors. Hence, it is not an intrinsic property of the TIM, but, rather, depends upon the details of the application.

Bruce Guenin, PhD

Bruce Guenin, PhD, is Principal Hardware Engineer at Oracle, San Diego, CA. He also serves as the Technical Editor of Electronics Cooling print edition and is no stranger to the readers of this magazine –Calculation Corner articles he has contributed are quite popular among thermal management professionals! Previously he served as Director of Thermal Characterization at Amkor Technology. He has devoted the past 27 years to all aspects of the thermal management and characterization of semiconductor components. In addition to his own technical contributions to innovation in component design, testing and simulation, he has been heavily involved in the dissemination of best practices in the industry through leadership positions in thermal conferences and standards committees. Dr. Guenin served as Chairman of the JEDEC JC-15 Committee for 15 years until 2014.

MATHEMATICAL REPRESENTATION

Assuming a 1-D heat flow, the thermal resistance of a TIM, including the two interfacial regions, is calculated from where A is the cross-sectional area of the TIM, t is its thickness (commonly referred to as the bond line thickness or BLT), K is its bulk thermal conductivity, Θ_{INT1} and Θ_{INT2} are the values of interfacial thermal resistance for unit area at each of the interfaces[1]. Θ_{INT} lumps both interfacial thermal resistances into a single value. Θ_{INT} is represented in metric units as cm2°C/W. *Equation 1* indicates that Θ_{TIM} is a linear function of the BLT, with a slope equal to 1/(AK) and a y-intercept equal to Θ_{INT}/A.

$$\Theta_{TIM} = \frac{1}{A} * \left(\frac{t}{\kappa} + \Theta_{INT1} + \Theta_{INT2}\right) = \frac{1}{A} * \left(\frac{t}{\kappa} + \Theta_{INT}\right) \quad (1)$$

Figure 2 illustrates the use of *Equation 1*. When Θ_{TIM} is measured using a series of test coupons with various TIM thicknesses, a line can be fitted to the resultant data. K and Θ_{INT} can then be determined directly from the slope and intercept.

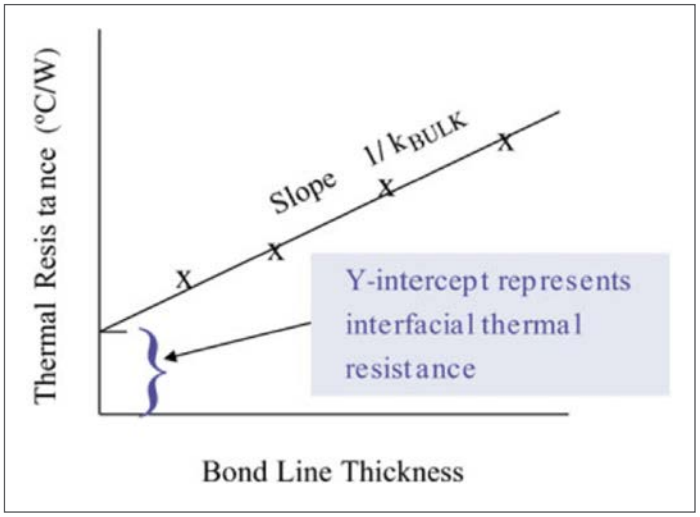


Figure 2. TIM thermal resistance versus bond line thickness.

CAUTIONARY NOTES

Note 1. Performing a series of measurements to extract the slope and intercept of Θ_{TIM} versus BLT can represent a significant effort. It is sometimes expedient to perform a measurement at one BLT value only. The equation $\Theta_{TIM} = t/AK_{EFF}$ is solved to yield a value of K_{EFF} (effective value of thermal conductivity). K_{EFF} can be used to calculate the temperature difference across a TIM with full accuracy only at the thickness at which it was measured. If EFF is used in calculations for the same TIM but at another value of BLT, significant error may result.

Note 2. TIM manufacturers who follow the established ASTM procedure will report only K for a particular material and not Θ_{INT}[2]. Their rationale is that, unlike K, Θ_{INT} can vary from application to application, and, hence, they have limited control over it. It is their policy to report on the properties that they have full control over and can be incorporated into specifications for the TIMs.

The ASTM procedure used to extract K is essentially that illustrated in *Figure 2*. As such it is rigorous, unlike the K_{EFF} method. Unfortunately, unless an appropriate value of Θ_{INT} can be included in TIM thermal calculations, considerable error may result, particularly at small values of BLT.

CONCLUSIONS

It is a straightforward procedure to calculate the thermal performance of a TIM as long as Θ_{INT} is properly accounted for. The biggest challenge can often be getting the correct values of K and Θ_{INT}

REFERENCES

[1] Solbrekken, G., Chiu, C-P, Byers, B., and Reichenbacker, D., "The Development of a Tool to Predict Package Level Thermal Interface Material Performance," Proceedings, ITherm Conference, May, 2000, pp. 48 – 54.

[2] ASTM Standard D5470-01, "Standard Test Methods for Thermal Transmission Properties of Thin Thermally Conductive Solid Electrical Insulation Materials." Available for purchase at www.astm.org.

Historical Suggestions for Thermal Management of Electronics

Jim Wilson
Engineering Fellow, Raytheon Company

I have a small book in my office labeled "*Suggestions for Designers of Navy Electronic Equipment, 1970 Edition*" and it was given to me several years ago by the editor at microwaves101.com (which happens to be a useful website if you are interested in microwave topics). The introduction states that any or all of this information is reproducible as long as credit lines are given, so a few pages related to thermal management (including the nice illustrations) are reproduced in this column.

An appropriate fact would be that thermal issues with electronics have been around as long as we have had electronics, but despite the long history of thermal management hardware and packaging solutions, it would be a fairy tale to think that cooling of electronics is easy. The suggestions in the book cover a range of topics that were of interest to end users of that time period such as design and reliability.

The book has 99 suggestions in the thermal section and perhaps not surprisingly, some of them still apply. This information was compiled before modeling and simulation was common or even practical with the computational resources of that time period.

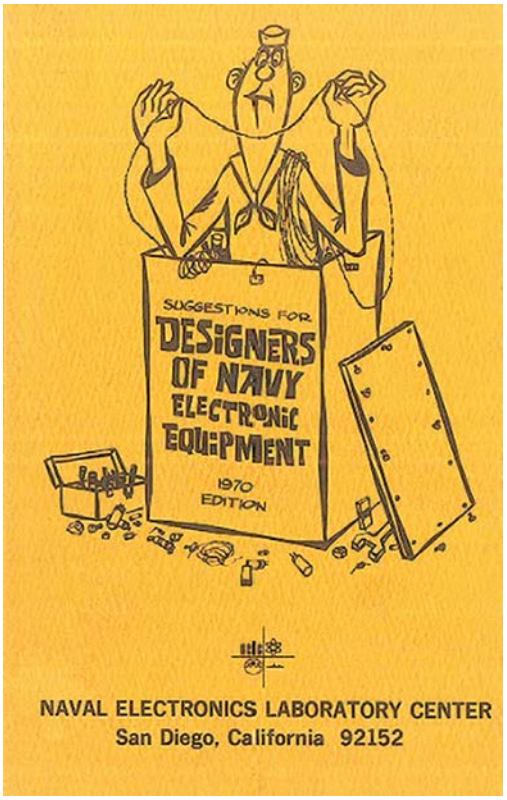
Expectations in 1970 relied on following generally accepted design practices and validation testing. Reasonable expectations of today are usually much more comprehensive and include simulations and confirmation tests. Densely packaged electronics with high heat loads that are common today would be difficult, if not impossible, to design without thermal simulation tools (and a thermal engineer to generate and interpret results).

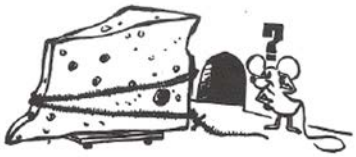
The thermal section starts with rough guidelines on selecting natural, forced air, liquid or two-phase cooling based on heat flux. Advances in packaging and heat sink designs have made air and liquid cooling feasible at higher heat flux levels for both free and forced convection.

General guidelines to consider when designing for natural, forced air, liquid, or vaporization cooling follow. The last suggestions are related to different types of electronics and while not many of us deal with tube cooling today, it is interesting to look at the integrated and other semiconductor devices section. Suggestion number 84 states that the thermal design of ICs are critical.

This statement has proven to be true and is one of the main focus topics of electronics cooling. Suggestion 95 comments on validating parameters listed in manufacturer's data sheets as they were found to be unreliable. Today, 45 years later, this is still good advice.

In the field of electronics thermal management, we have significantly more design capability today than existed when this book was compiled. However, a good lesson for all of us is to remember that this book was written from the end user's viewpoint. We should make sure that considering the customer's perspective in our thermal management designs has a high priority.





41. Ensure that equipment enclosures meet requirement 55 of MIL-STD-454B[9] to the degree required in the individual equipment specifications.
42. Design for MIL-E-16400F[3] extreme environmental requirements (may be modified by equipment specifications): (3.8)
    a. −62 degrees to +75 degrees C (non-operating).
    b. −54 degrees to +65 degrees C (operating), as defined by the equipment specification.
    c. 95 percent relative humidity.
    d. Equipment exposed to weather is expected to withstand winds of 100 knots and to operate in winds of 75 knots.
    e. Equipment exposed to weather should operate with an ice load of 4.5 pounds per square foot.

30

f. Equipment should withstand shock and vibration (MIL-S-901C[16] and MIL-STD-167A Type I[17]). (4.5.14)
g. Equipment should withstand salt spray (for external finishes and materials). (FED-STD-151 Method 811[18]) (4.5.15)

THERMAL[19]

1. The choice of a cooling means for an electronic equipment depends on the heat dissipation density in the unit:
    a. Use natural cooling (free conduction, convection, radiation) when the heat dissipation density in the unit is less than 0.25 watt per square inch.
    b. For heat dissipation density from 0.25 to 2 watts per square inch, forced-air cooling is recommended.
    c. Employ liquid or vaporization cooling if the dissipation density in a unit is over 2 watts per square inch.
2. For most miniaturized electronic assemblies, natural cooling is frequently the only practical means of heat transfer within equipment.
3. Of the three modes of heat transfer in natural cooling, metallic conduction is recommended as the primary cooling means.

31

4. For electronic equipment designed to operate in thermal environment of high ambient temperature or with high heat dissipations, liquid or vaporization cooling is best.
5. Base the design of forced-air cooling systems on the volume and weight of the equipment, the attainment of safe operating temperature at the heat sources, and the minimization of cooling power; i.e., the energy requirement for moving the air through the cooling system.

32

6. Limit heat dissipation by choosing efficient parts (semiconductor devices instead of electron tubes, for example) and circuits (class B or C operation instead of class A).
7. Use parts which have maximum thermal operating range and minimum temperature sensitivity.
8. Design circuits to be as tolerant of temperature range as possible. NEVER assume that a design will be satisfactory over the range of temperatures required of military equipment on the basis of tests performed at room ambient temperature on a development bench.
9. Design equipment so that heat flow paths are the result of planned effort in order that thermal performance may be subject to manufacturing control in the same manner as electrical performance.

NATURAL COOLING[20,21]

10. Use heat flow paths of lowest possible thermal resistance.
11. Ensure that heat flow paths are as short as possible, have large cross-sectional areas, and are made of material having good thermal conductivity.

33

12. Arrange hot components to form a bank of minimum height.
13. Use heavy metal chassis for conducting heat.
14. Stagger parts where vertical stacking is used.
15. Make sure all joints conduct heat well and are close fitting to provide a maximum metal-to-metal contact. Where necessary, silicon greases are recommended for use in improving joint conductivity.
16. Isolate from or place below heat sources all temperature-sensitive components.
17. Provide polished and unpainted heat shields for heat-sensitive components located less than 2 inches from heat source.
18. Mount all parts which dissipate more than 1/2 watt on metal chassis or provide them with heat paths leading to a heat sink.

34

19. Provide ventilation louvers of proper design and location that will provide a drip-proof enclosure where required.
20. Make sure that heat sources have high emissivity and, if embedded, are provided with metal heat conductors.

FORCED-AIR COOLING[22]

21. Direct cooled, filtered air to the hot parts.
22. Avoid reuse of cooling air. If secondhand air or series-flow air must be used, the sequence of air passage over cooled parts must be carefully planned so that temperature-sensitive parts or parts with low maximum permissible operating temperatures are cooled first, and so that the coolant has sufficient thermal capacity to maintain required temperature for all parts.
23. Cool hot parts by parallel air flow.
24. Insure the air flow paths are free and unobstructed and are of proper size.
25. Insure that intakes and exhausts are far apart.
26. Design so that the blower capacity is adequate and blower motor is cooled.
27. Verify air flow in equipment by measuring and mapping with smoke.
28. Make air filters adequate and accessible for easy cleaning and replacement.
29. Consider protecting against equipment damage in case of blower failure.
30. Insure that power tubes have required air flow.

35

31. Minimize air-flow noise.
32. Measure the critical temperatures and protect fragile fins.
33. Design to have the air flow first pass over the seals of critical tubes.
34. Design so that forced convection is in a direction to aid the natural convection.
35. Include in air-flow calculations area reduction caused by wiring (including ship wiring) in the air ducts.
36. Do not locate ventilation openings at enclosure top, bottom, or front surfaces without specific approval.

LIQUID COOLING[23]

36

37. Obtain approval of the command or agency concerned if liquid cooling is used.
38. Design so that the coolant can expand freely and the enclosure can withstand the maximum vapor pressure of the coolant.
39. Be sure that the piping is adequate and equipment is hermetically sealed.
40. Provide adequate drains and filter plugs.
41. Design equipment so that drains are at low points and bleeder valves are at high points of the system.
42. Insure that the heat exchangers are of proper design and capacity.
43. Insure that the coolant does not boil below maximum temperature and, if necessary, provide a temperature control device.
44. Avoid condensation of moisture in the equipment. But if it happens to be unavoidable, a pressure of nearly one atmosphere should be maintained outside of the enclosure.
45. Use a check valve at each disconnection.
46. Orient and mount parts to achieve maximum convection.
47. If feasible, design to provide metallic conduction paths of low thermal resistance from heat sources to the case; although they are not essential, they are very helpful and do not require special attention.
48. In designing the cooling assembly always remember the aspects of maintenance and repair.

37

VAPORIZATION COOLING[23]

(Factors applicable to liquid cooling apply here also.)

49. Be sure that sufficient coolant is provided.
50. If required, install a make-up reservoir.
51. Prevent toxic fumes from reaching personnel.
52. Provide pressure control and pressure relief valves.
53. Conduct environmental tests on refrigeration systems.

COOLING OF TUBES[5]

54. Position electron tubes so as to avoid the formation of hot spots.
55. Space unshielded tubes at least 1-1/2 diameter apart.
56. Screen tubes from each other; do not pot tubes in plastics.
57. Avoid direct radiation from electron tubes.
58. Avoid running tube anodes red hot.
59. Verify that the bulb temperatures are within specification.
60. Protect tubes from mechanical injury.
61. Use thermocouples or temperature sensitive paints to investigate thermally critical tube applications.

TUBE SHIELDS

62. Use nonmagnetic heat dissipating shields on all miniature and subminiature tubes. (3.4.33)
63. Make shields fit the tubes tightly; use non-precious metals.

38

64. Choose shields that are highly emissive and thermally conductive to the chassis.
65. Provide low-resistance metal joints.
66. Avoid mounting heat-conducting shields on plastic chassis.
67. Use shields that have been blackened internally and polished externally.

RESISTORS (which dissipate more than 1/10 rated power)

68. Bond resistors to the panel or chassis by a clamp of low thermal resistance.
69. Do not place resistors adjacent to heat-sensitive components.
70. Mount power resistors vertically in groups. Similarly mount other resistors over 5 inches long.
71. Mount resistors so that leads are as short as possible.
72. Design to allow air to flow freely over resistors.
73. Derate resistors if environmental temperatures are high, in accordance with tables established in the applicable specifications. A minimum derating of 50 percent is normal.
74. Locate composition resistors, such as those used in feedback loops or bridge-balancing networks, in comparatively cool areas.
75. Place bleeder resistors adjacent to cabinet or chassis surfaces that provide good thermal sinks.

39

CAPACITORS

76. Isolate heat-sensitive capacitors from hot components.
77. Provide radiation shields.
78. If possible, use capacitors or relatively low-heat-sensitivity materials.

TRANSFORMERS AND INDUCTORS

79. Provide transformers and chokes with clean low-resistance thermal joints to heat-conducting chassis.
80. Keep transformers potted and enclosed.
81. Provide adequate heat dissipation surface areas and good thermal conductivity between the windings and case.
82. Make sure that thermal joints are free of impregnant and paint.
83. Isolate temperature-sensitive inductors from heat sources; if possible, locate them near a cabinet or other metallic thermal sink.

INTEGRATED CIRCUITS AND OTHER SEMICONDUCTOR DEVICES

84. Remember that semiconductor devices are usually very heat sensitive. Thus, their thermal designs are critical.
85. If power transistors or power rectifiers are used, provide connections of low thermal resistance to well-cooled, heat-conducting chassis.

40

86. Keep temperature environment as nearly constant as possible.
87. Clamp transistors dissipating more than 100 milliwatts to a chassis or heat sink.
88. Mount power rectifiers in a cool place and provide them with large, vertical fins.
89. Design to insure that semiconductor devices will not deteriorate in performance with increasing temperature.
90. The use of solder is preferred for mounting of integrated circuits to boards. In any case, sockets should not be used because of their unreliability. The use of welding is not recommended since repairs often damage circuit board conductors and in addition create quality control problems related to welding schedules, etc.
91. Mount integrated circuits so that the case firmly contacts the mounting surface to provide heat sinking.
92. Do not mount integrated circuits by suspending them from their leads.
93. Do not rely entirely on heat sinking. Integrated circuits require additional cooling.

41

94. Use only integrated circuits with gold-plated leads. In addition, the leads must have been plated prior to sealing the case. The use of conformal coatings to seal assemblies is encouraged, since leads are generally Kovar and rust rapidly. Consideration must be given to use of coatings which will facilitate repair if this is part of the maintenance philosophy.
95. Critically screen manfuacturer's electrical parameter values, as these values quite frequently are unrealistic and optimistic. It is recommended that circuits be tested to determine typical values.
96. Do not load integrated circuit outputs to more than 70 percent of manufacturer's maximum fanout ratings.
97. Do not exceed the manufacturer's recommended power supply voltage. Maximum ratings should never be used. Guard against electromagnetic interference by use of appropriate shielding. Integrated circuits are susceptible to and create noise.
98. Do not use edge board connectors with less than 0.100 inch contact spacing for mounting integrated circuits. Less spacing provides insufficient contact area and reduces reliability.

99. The use of wire-wrap in accordance with MIL-STD-1130[24] provides acceptable back plane wiring. Solder terminations with sufficient quality control generally result in acceptable wiring. Any other termination should be subjected to critical screening through environmental evaluations, as well as maintenance tests prior to selection and usage.

Solder Joint Lifetime of Rapidly Cycled LED Components

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INTRODUCTION

Active leds in a consumer TV product are boosted and dimmed with the video picture content. Boosting and dimming of LEDs is a powerful means to improve visual experience, either through application of active LEDs in an ambient light feature, or through dimming and boosting of the display LEDs in a direct lit video display. Active driving of LEDs is also a significant consideration in the thermal management of a video display product[1, 2]. However, active driving of LEDs increases the number of temperature cycles by several orders of magnitude, and thermal cycling is well known to lead to so-called low cycle fatigue solder joint failure. How then will active driving of LEDs affect the lifetime of LED solder joints in a TV product?

SOLDER FATIGUE AT LONG TIME SCALE

The root cause of low cycle fatigue solder joint failure is that thermal mismatch between a component and PCB is taken up in deformation of the solder joint. Assume that a SMD LED is subjected to an instantaneous temperature rise ΔT at t=0 s. This results in a thermal shear strain εT in the solder joint, proportional to the temperature change, $\varepsilon_T \sim \Delta T$. At t=0s, the entire thermal strain is taken elastically. By Hooke's law, the shear stress σ is proportional to the elastic strain ε_e with proportionality constant G, the solder's shear modulus G= 2(E1+v) . Thus, at the instantaneous temperature rise $\sigma_0 = G \cdot \varepsilon_e = G \cdot \varepsilon_T$. At longer times the solder starts to creep, that is, to flow very slowly, and part of the thermal strain is taken in creep strain ε_c. This lowers the elastic strain and the stress relaxes.

$$\sigma = G \cdot \varepsilon_e = G \cdot (\varepsilon_T - \varepsilon_c) \quad (1)$$

When the creep strain equals the thermal strain, $\varepsilon_c = \varepsilon_T$, the elastic strain is zero and the joint is stress-free. If the temperature is then lowered by -ΔT, the change of temperature with respect to the stress-free situation will again cause a thermal mismatch, which will again cause stress in the solder joint,$-\sigma_0$, which will again relax away to the stress-free situation through solder creep. In this manner, temperature cycles result in cyclic loading, creep and stress relaxation in the solder joint. The diagram of stress versus creep strain is shown in *Figure 1*.

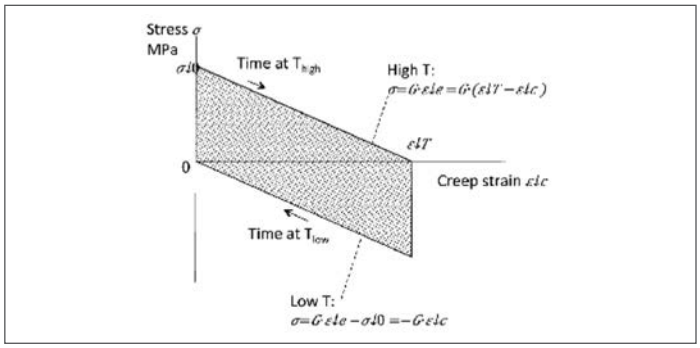

Figure 1. Stress-creep strain loop from cyclic thermal load.

In each cycle, an amount of damage is incurred that is proportional to the area inside the stress-creep strain loop. Solder joint failure occurs once the total accumulated creep damage exceeds a certain value C, which is usually determined through an accelerated test. *Figure 1* shows that the area inside the loop for a full creep cycle up to the stress free situation equals $\sigma_0 \cdot \varepsilon_T$. It follows that the area of the loop is proportional to ΔT^2:

$$\text{Area} = \sigma_0 \cdot \varepsilon_T = G \cdot \varepsilon_T^2 \sim \Delta T^2 \quad (2)$$

A similar relationship is also found in the low-cycle fatigue law of Coffin-Manson[4], in the work of Engelmaier [5, 6] and of Norris-Landzberg[10] in the form of fatigue exponent, which roughly corresponds to a value 2. The quadratic dependency is also the basis for the common design rule relating the number of cycles to failure in operation N_f to the number of cycles to failure Ntest in

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an accelerated test with temperature sweep ΔT_{test}:

$$N_f = \frac{N_{test}(\Delta T_{test})^2}{\Delta T^2} \quad (3)$$

The fatigue cycle shown in *Figure 1* will only appear if the heating and cooling is instantaneous, and if dwell times are sufficiently long to allow for relaxation up to the stress free situation. It is well-known that the durations of ramp time and dwell time have a significant impact in accelerated temperature cycle tests[7]. Both the Engelmaijer and the Norris-Landzberg model incorporate the effect of field vs. test timing in a time factor in their models. However, it is not obvious that these models are appropriate for short video time cycles. Typical temperature cycle tests have at most one order of magnitude difference from test to field condition. Since temperature effects dominate the acceleration factors, it then becomes difficult to separate out time effects with accuracy. Furthermore lifetime, test timing parameters and test temperatures are interrelated in a complex manner[10]; therefore, separation of time and temperature effects does not lend itself to extrapolating with confidence. As an example, the Engelmaijer relations were critically reviewed in[8] and shown not to be reliable for several cases. Hence using existing simple models incorporating the cycle time effects is not straightforward for short video cycles and more accurate numerical investigation using FEMare often not possible in view of limited project resources.

Table 1. SAC Material Properties

Parameter	Value	Unit
Schubert model		
A	277984	s^{-1}
B	0.02447	MPa^{-1}
C	6.41	
D	6500	K^{-1}
Elastic constants		
E	61251–58.5 T	MPa, T in Kelvin
v	0.36	

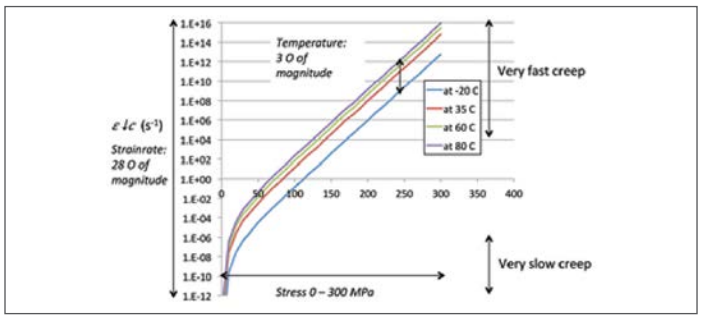

Figure 2. Creep strain rate ε ↓ c(s^{-1}) as a function of stress ε(MPa).

SOLDER FATIGUE AT SHORT TIME SCALE

The purpose of the current work is to find out the influence of short cycle times on solder failure in a less resource-intensive manner, allowing for a better lifetime estimate in a safe engineering envelope. Direct integration of the creep strain rate is used to determine how much creep will actually occur in the cycle time.

The flow rate or creep strain rate of solder is extremely dependant on stress and temperature. According to Syed's formulation of the Schubert model for lead-free solder[9], the creep strain rate is the product of a stress dependent part $g(\sigma)$ and a temperature dependent part $f(T)$.

$$g(\sigma) = A\{\sinh(B\sigma)\}^C \quad (4)$$

$$f(T) = \exp\left(\frac{D}{T}\right) \quad (5)$$

$$\dot{\varepsilon}_c = g(\sigma)f(T) = A\{sinh(B\sigma)\}^C \, exp\left(\frac{D}{T}\right) \quad (6)$$

Table 1 shows the values for the material parameters A through D, as well as the elastic modulus E and Poisson ratio ν.

Figure 2 shows the calculated creep strain rates for a -20 °C to 85 °C temperature range and 0 – 300 Pa stress range.

It shows that the shear strain rate varies 28 orders of magnitude over the stress range. At high stress levels, the extremely high creep strain rate will immediately relax the stress to a lower level, so this part of the stress relaxation does not cost significant time. At low stresses, the very low creep rate will result in negligible creep in the time range of 1 – 104 s. *Figure 2* also shows that the creep strain rate varies three orders of magnitude in the temperature range -20 °C to +80 °C. In contrast, from *Table 1*, the variation in the elastic modulus over the same temperature range is only 14%. Therefore, in all subsequent calculations the shear modulus will be taken at the mean temperature of the high and the low temperature.

Total creep in the cycle time is closely coupled to the amount of stress relaxation. The stress relaxation curves at a certain temperature are obtained in the following way:

The shear stress is proportional to the shear strain. Taking the time derivative of *Equation 1* and substituting *Equation 6*:

$$\dot{\sigma} = -G\dot{\varepsilon}_c = -G \cdot g(\sigma)f(T) \quad (7)$$

For sufficiently small increments Δσ, this can be used to find the time that it takes to realize the stress increment.

$$\Delta t = \frac{\Delta\sigma}{\dot{\sigma}} \quad (8)$$

Summing the time increments associated with the stress increments results in an approximation of the stress relaxation over time. The whole scheme is easily implemented in a spreadsheet, as shown in *Figure 3*. The corresponding stress relaxation curves at -20 °C and +85 °C are shown in *Figure 4*. Similar curves can be made for different initial stress levels and different temperatures, and these are used to determine how much stress relaxation will take place in a certain creep time. Subsequently the stress-creep strain cycle can be constructed.

$\varepsilon\downarrow c(\sigma)$ from Schubert model

$$\sigma = G \cdot \varepsilon\downarrow e = G \cdot (\varepsilon\downarrow T - \varepsilon\downarrow c)$$

$$\downarrow$$

$$\sigma = -G\varepsilon\downarrow c$$

$$dt = \Delta\sigma/\dot{\sigma}$$

$$t = \Sigma dt$$

$$\downarrow$$

$$\sigma(t)$$

Figure 3. Spreadsheet Implimentation

T (C)	-20			85		
T (K)	253			358		
G (Tavg)	15949			15949		
strainrate T part	6.95403E-12			1.30246E-08		
shearstress	stress rate	dt	t-cumulative	stress rate	dt	t-cumulative
MPa	MPa/s	s	s	MPa/s		
152	8.17E+06	2.69E-06	2.69E-06	1.53E+10	1.44E-09	1.44E-09
130	2.57E+05	3.89E-05	4.16E-05	4.82E+08	2.08E-08	2.22E-08
120	5.32E+04	1.88E-04	2.30E-04	9.96E+07	1.00E-07	1.23E-07
110	1.10E+04	9.13E-04	1.14E-03	2.05E+07	4.87E-07	6.10E-07
100	2.24E+03	4.46E-03	5.60E-03	4.20E+06	2.38E-06	2.99E-06
90	4.53E+02	2.21E-02	2.77E-02	8.48E+05	1.18E-05	1.48E-05
80	8.97E+01	1.11E-01	1.39E-01	1.68E+05	5.95E-05	7.43E-05
70	1.72E+01	5.81E-01	7.20E-01	3.22E+04	3.10E-04	3.85E-04
60	3.12E+00	3.20E+00	3.92E+00	5.85E+03	1.71E-03	2.09E-03
50	5.17E-01	1.93E+01	2.33E+01	9.68E+02	1.03E-02	1.24E-02
40	7.25E-02	1.38E+02	1.61E+02	1.36E+02	7.36E-02	8.61E-02
30	7.48E-03	1.34E+03	1.50E+03	1.40E+01	7.13E-01	7.99E-01
20	4.07E-04	1.23E+04	1.38E+04	7.63E-01	6.55E+00	7.35E+00
15	5.77E-05	8.67E+04	1.00E+05	1.08E-01	4.63E+01	5.36E+01
10	3.96E-06	5.05E+05	6.05E+05	7.42E-03	2.70E+02	3.23E+02
8	9.26E-07	2.16E+06	2.77E+06	1.73E-03	1.15E+03	1.48E+03
6	1.44E-07	1.39E+07	1.67E+07	2.69E-04	7.42E+03	8.90E+03
4	1.06E-08	1.89E+08	2.06E+08	1.98E-05	1.01E+05	1.10E+05
2	1.23E-10	1.62E+10	1.64E+10	2.31E-07	8.66E+06	8.77E+06

Figure 3. Spreadsheet implementation

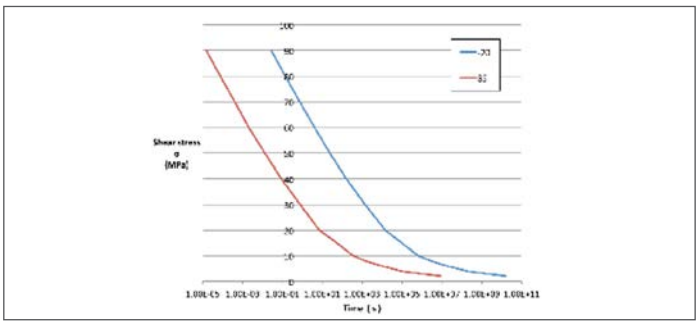

Figure 4. Stress relaxation curves at -20 °C and +85 °C.

VIDEO LED APPLICATION

We consider an idealized temperature cycle with instantaneous temperature change and an equal time at the high and at the low temperature. Four cases are of interest: a) the accelerated test, b) the on/off cycle, c) a long 100 s video cycle, and d) a short 5 s video cycle. *Figure 5* shows the calculated stress/creep strain cycles and *Table 2* the load case details and resulting creep strain.

Table 2. Load Cases

		T_{low}	T_{high}	creep time	ΔT	ε_T	σ_0	% full creep
case		C	C	s	C		MPa	
a	Accelerated test	-20	85	3000	105	0.95%	152	79%
b	on/off	35	80	3600	45	0.41%	63	71%
c	long boost	60	90	100	30	0.27%	41	37%
d	short boost	60	80	5	20	0.18%	27	0%

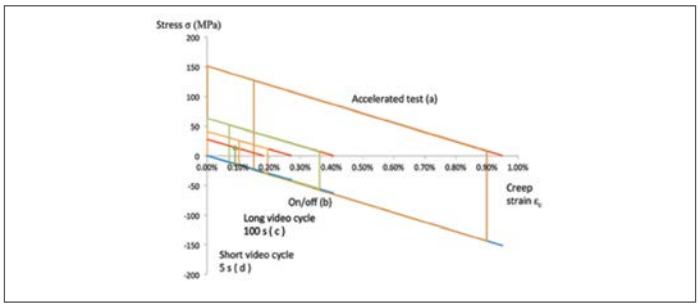

Figure 5. Stress – creep strain loops

In all cases, even in the accelerated test, creep times turn out to be too short for full creep to occur. *Figure 5* and *Table 2* show that using a large temperature step in the accelerated test case works out like intended: the area of the test cycle is much larger compared to the use cycles, thus failure will be accelerated and the failure energy value can be obtained in shorter time. Creep in the on/off cycle case is slightly less complete compared to the accelerated case, therefore using the accelerated test to predict the number of cycles to failure as per the normal design rule in *Equation 3* works out well with a sensible engineering margin of (79/71-1)=11%. This is not the case for the video cycles. Not taking the short time effect into account leads to roughly a factor 2 underestimation in lifetime for the long video cycle. In case of the short video cycle, the temperature excursions are all taken elastically, no creep damage is incurred and use of *Equation 3* is not appropriate at all. This shows that for short cycle times the time effect must be taken into account for correct lifetime prediction of the solder joints.

SUMMARY AND CONCLUSION

The effect of short creep time on low cycle fatigue failure of SMD LEDs was investigated. It was shown that for an idealized case with instantaneous temperature change, full creep i.e. stress relaxation to the stress free level and with temperature independent elastic moduli, the creep damage per cycle is proportional to $\Delta T2$. Direct integration was used to construct stress relaxation curves incorporating the highly non-linear behavior of the lead free solder as per the Syed/Schubert model; these were used to construct a simplified stress-strain fatigue cycle, incorporating the effect of creep time. Application to active LEDs in a TV product demonstrated the validity of accelerated testing and the $\Delta T2$ design rule to product on/off cycles. In contrast, this was not the case for the typical video cycle times. The short cycle times only allow for partial creep, doing less damage per cycle, and so the use of the uncorrected design rule leads to under prediction of solder joint lifetime. At

very short cycle times, the cyclic thermal mismatch is taken fully in elastic excursions with no creep at all, and low cycle fatigue is not the appropriate failure mode. Although the complexity of the solder joint fatigue cycle was very much simplified in the work, the approach was shown to be of merit in clarifying main effects in low cycle solder fatigue, and in enabling correct first order engineering estimations using only a commercial spreadsheet.

ACKNOWLEDGMENTS

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A Figure of Merit for Smart Phone Thermal Management

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Jon J. Anderson received his B.S. and M.S. degrees in Electrical Engineering from Kansas State University, Manhattan, KS. In 1996, he joined Qualcomm Incorporated in Boulder, Colorado, where he is a Senior Director of Engineering. At Qualcomm, he leads all the thermal related engineering activities, including architecture, analysis, measurement, control and customer engineering. Prior to this thermal role, he conducted CDMA physical layer studies in terrestrial and satellite communication systems. Before joining Qualcomm, Jon was an officer in the US Air Force, working in the Space Experiments Division of Phillips Laboratory at Kirtland AFB, NM. He holds 36 patents with an additional 14 pending.

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INTRODUCTION

With smart phones and other mobile devices available in a variety of sizes and shapes, it is challenging to think in a consistent and comparative manner about the effectiveness of the thermal management solutions that they employ. This is growing more important as the mobile and wireless industries and associated research communities explore novel mobile cooling approaches. Here we define a universal thermal figure of merit - a dimensionless Coefficient of Thermal Spreading (CTS) – that can be calculated using either numerical simulations or Infrared (IR) surface temperature imaging and can be used to compare the thermal design effectiveness of many mobile devices and power levels. The proposed CTS Figure of Merit quantifies the effectiveness of heat spreading within the device by means of the uniformity of the surface temperature, and addresses a long-time need to quantify the thermal design effectiveness of various mobile devices which are skin temperature limited.

There has been past work on thermal performance metrics of electronics, particularly those for which central processing unit (CPU) overheating limits power generation. Some metrics are defined at the package level for single or multi-chip designs, and are useful for junction temperature prediction and as performance figures of merit[1, 2]. Other authors discuss the importance of the skin cooling and other thermal challenges in handheld mobile devices[3, 4]. However, when it comes to the system level thermal performance, the industry lacks a metric to quantify the "goodness" of the thermal design. A key benefit of such a metric would be to track the impact of design changes on the thermal performance considering the device skin limits.

One major thermal challenge of portable electronic devices is the strong spatial and temporal variability of the thermal boundary conditions at the case. A phone with outstanding internal thermal management will likely aim for a reasonably consistent temperature on its exterior surfaces. In fact, in the limit of perfect internal thermal management, all of the heat generated by the chips and other components inside the phone will be spread to the various phone surfaces and provide a nearly uniform temperature distribution when viewed from the outside. *Figure 1* shows that selecting a good thermal management strategy inside the phone improves the temperature uniformity and lowers the peak surface temperature.

Figure 1 illustrates that phone thermal design must meet certain skin limit temperatures and avoid the potential hot spots. The poor heat spreading on the device surface leads to a peak temperature of 59.5oC (*Figure 1(b)*), violating the 45oC skin temperature limit specifications set for the current design. By improving the thermal spreading, the peak temperature drops below the critical limit (*Figure 1(a)*).

The new proposed spreading metric is important both for thermal and electrical design/performance. At present, to meet the various performance specifications (skin/junction limit temperatures), the processors are throttled to reduce the power that leads to exceeding the limits. It is in the interest of the chip/device manufacturers to come up with a system level solution that will increase the overall electrical and thermal performance. This prompted the need for a heat spreading metric.

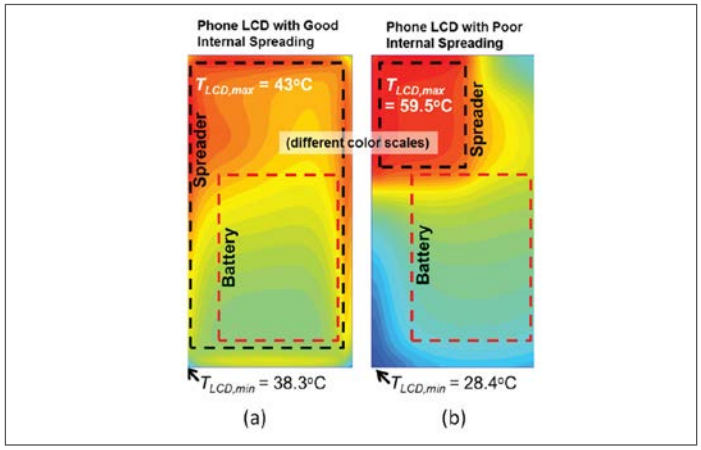


Figure 1. Simulated temperature distributions on the surface of a generic phone LCD (138 mm x 70 mm) for two different thermal management schemes. (a) Large heat spreader (128 mm x 62 mm), which couples the battery with the heat generating chips and yields a more uniform temperature. (b) Smaller heat spreader (35 mm x 33 mm) yielding highly non-uniform LCD temperature.

DEFINING THE COEFFICIENT OF THERMAL SPREADING (CTS)

We define the specific figure of merit associated with the heat spreading efficiency, a metric which we will call the "Coefficient of Thermal Spreading" (CTS). This metric indicates that by designing towards improvements in the CTS, we can improve the heat spreading and enhance the power handling capacity of a given phone/mobile device, achieving higher performance. *Figure 1* suggests that the variation of the surface temperature is decreased as the thermal design quality improves. One strategy for defining the CTS would be to evaluate the standard deviation of the temperature about its average value, Tave. The maximum temperatures depicted for the two phone designs in *Figure 1* suggest the following:

$$CTS = \frac{\theta_{ave}}{\theta_{\max}} = (T_{ave} - T_{ambient}) / (T_{max} - T_{ambient}) \quad (1)$$

Equation (1) is simply the ratio of the average temperature rise on the phone surface to the peak temperature rise. This ratio is dimensionless and increases to unity as the phone approaches a "perfect" thermal design, with uniform case temperature, for which Tave and Tmax are the same. In contrast to a metric based on the standard deviation, *Equation (1)* is directly related to power and maximum surface temperature, the key inputs/deliverables of the design process. Improving the CTS translates directly into a reduction of the maximum surface temperature for a given power.

To develop a quantitative metric, it is a useful to assume a constant value of the convective heat transfer coefficient, h, over the entire surface, in part because the local heat transfer rate varies due to a variety of external parameters. *Equation (2)* shows that for a given power and surface area, the average surface temperature is independent of the phone design. A poorly designed phone has hot/cold regions, but the average surface temperature is the same as of a well designed phone, assuming equal power generation and surface area for both devices.

$$P_{phone} = h\,A\,\theta_{ave} \quad (2)$$

where P_{phone} [W] is the total heat generated in the phone; A is the total surface area, and $\theta_{ave} = T_{ave} - T_{ambient}$ is the average phone surface temperature rise relative to the ambient air.

There is another way to calculate the CTS, which may be more straightforward depending on what information is available. Making use of *Equation (2)*, we calculate the CTS using:

$$\text{CTS} = \frac{P_{phone}}{hA\theta_{\max}} = \frac{P_{phone}}{P_{perfect}} \quad (3)$$

where P_{phone} is the power generated without rising above the case temperature limit and $P_{perfect/ideal}$ is the power removed from a phone with perfect internal spreading. *Equation (3)* is useful for extracting the CTS from infrared imaging data, which can provide a solid estimate of the maximum temperature rise.

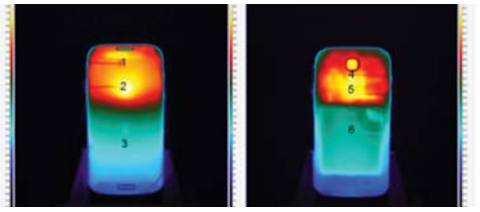
MEASURING THE CTS

IR imaging was performed to gain understanding of the CTS metric. The benchmark use case is Quad-Dhrystone and the device is in vertical orientation (*Figure 2(a)*). Test details/equipment: a) K-type thermocouple measures the ambient temperature; b) data logger records the thermocouples temperatures; c) IR camera measures the LCD/Back Cover peak/average temperatures; d) Wait 40 mins until surface temperatures reach steady-state, start CTS measurement.

Since the surface emissivity of LCD/back cover is unknown, three K-type thermocouples (designated as 1 through 6, three on each LCD/Back cover surface) were mounted at low/medium/high-temperature zones at LCD/Back cover (*Figure 2(b)*). The thermocouple readings were used as the reference temperature to calibrate the emissivity of the LCD/Back cover surfaces. The surface emissivity setting of the IR camera is adjusted until the temperature difference between the thermocouple and IR camera reading is less than 1°C. The determined surface emissivity is the emissivity of the LCD/Back cover surface. There is potential for further reduction in the tests variability (due to the open air environment) by using JEDEC closed box[5], with modified port for IR camera access. This deserves further evaluation, in case the industry is moving towards the CTS concept adoption.

To capture the temperature profiles: a) Run power intensive use case; b) Capture the surface temperature using IR camera; c) Port the IR temperature data into .csv file; d) Do an area weighted average of the surface temperatures for the display/case surfaces; e) Extract the overall device skin maximum temperature; f) Calculate CTS = $(T_{ave,\ skin} - T_{ambient})/(T_{max,\ skin} - T_{ambient})$. *Figure 3* summarizes the CTS measurement over 30 minute: CTS peaks at 0.62 for this specific device.

a) Test set up



b) Measured IR thermographs

Figure 2. IR imaging of commercial phone.
Note Thermocouple locations 1 to 6 defined in (b)

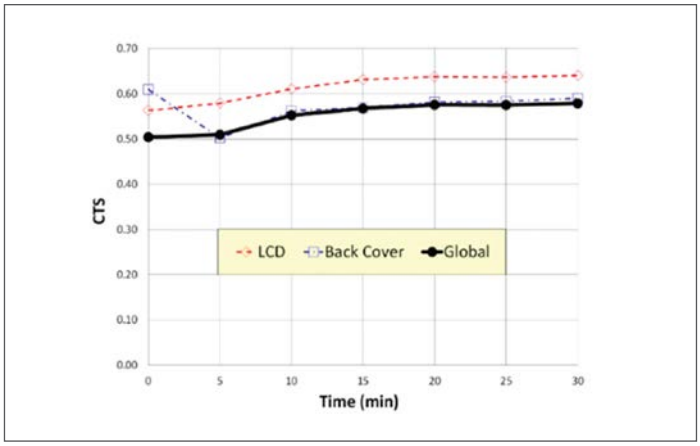


Figure 3. Calculated Coefficient of Thermal Spreading extracted experimentally for commercial phone.

EXAMPLE APPLICATIONS OF THE COEFFICIENT OF THERMAL SPREADING (CTS)

We expect the CTS to guide the design improvements and interactions with the phone/mobile manufacturers/companies. We completed several simulation/CFD studies of phone design incorporating differing spreader geometries, at various powers. *Figure 4* plots the simulated maximum surface temperatures as a function of heat spreader geometry and power.

For a phone that is cooled sufficiently well, increasing the CTS guides to higher power capacity without overheating the case. In *Figure 4*, the green arrow draws attention to three successive simulations for increasing spreader size that allow the power to be increased from 2.2 to 3.5 W without overheating the skin. Larger spreaders allow the CTS to increase from 0.5 to 0.8. By increasing the CTS of a device from 0.5 to 0.8, there is over 1.2W Power benefit and the skin limit stays at 45oC.

For problem phone designs (device skin is too hot), increasing the CTS should guide to a working design, or to the conclusion that the power is unmanageable. The blue arrow in *Figure 4* draws attention to three successive simulations at 3.5W constant power, for which increasing the spreader size (thus increasing the CTS) drops the maximum skin temperature from ~ 60oC to the required 45oC limit.

For the case of 6.7W and the big spreader, the red arrow suggests that the CTS needs to be increased above unity to function properly. This is impossible, as the CTS reaches a maximum of one for a perfect/isothermal case, meaning that power reductions will be essential. For that specific device platform, the maximum power using an ideal CTS is limited to 3.8W.

Finally, the CTS is a figure of merit for the design geometries/materials, and should be independent of the power level for the given use case/s. The dashed blue lines in *Figure 4* show that, for a given spreader dimension, the CTS is essentially independent of the phone power. The dashed lines are not perfectly vertical because of the slight temperature dependence of the thermal properties.

Although the CTS is power independent for specific use case/s, the CTS does vary with time. If *Equation (1)* is evaluated as a function of time, while the device is heating up, the CTS evolves with time and approaches higher degree of uniformity in steady state. The CTS remains largely independent of power levels, although this can become more complicated if the power is time varying as well.

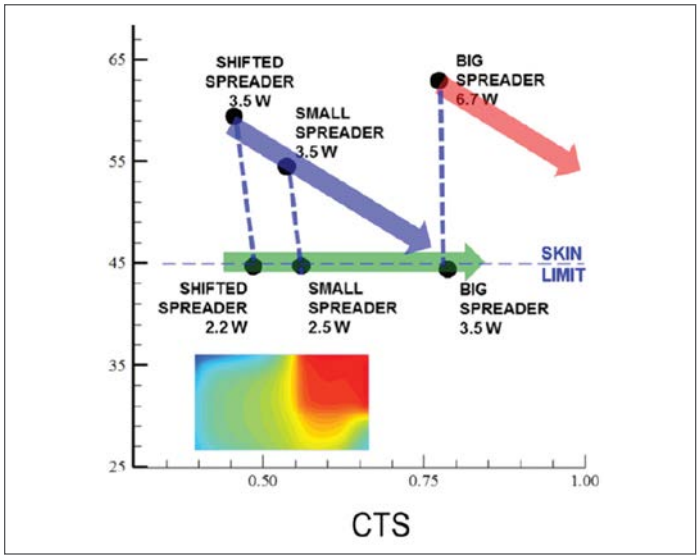


Figure 4. Maximum skin temperature versus CTS. Note: (i) The phone designs along the green arrow are limited by skin temperature, with power chosen specifically to meet that limit. (ii) The designs along the blue arrow show what happens to the skin temperature, for a constant given power, through improved thermal design. (iii) The red arrow suggests that it is impossible to improve a design sufficiently to cool very large power loads.

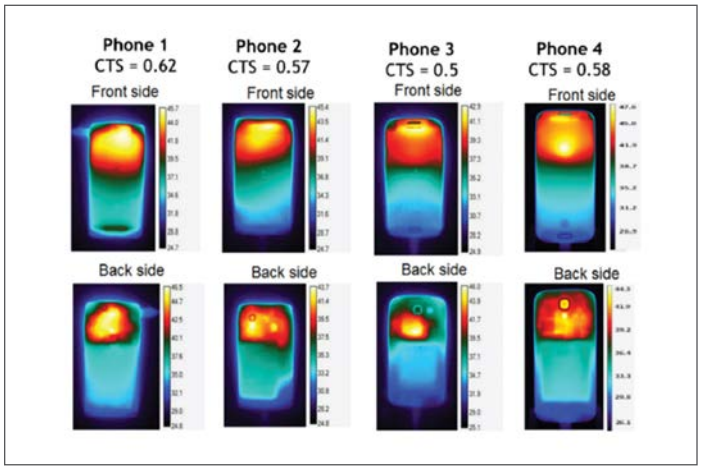


Figure 5. Measured IR temperature surface thermographs and CTS values for several commercial phones. CTS calculated using Equation (3) and the infrared imaging data. The temperature scale is different for each phone.

QUANTITATIVE DESIGN TARGETS USING THE CTS

The CTS is a powerful tool as it enables the best performing mobile/portable electronic devices. Chip manufacturers can

define a minimally acceptable CTS level to ensure that their chips are cooled appropriately and deliver a level of performance that customers will find compelling/favorable. While all companies should strive for a CTS approaching unity (the perfectly cooled phone/mobile), eventually the costs associated with internal thermal management may become excessive. With improvements in thermal technologies, the higher CTS/performance devices should increase.

Our internal thermometry work has evaluated CTS values from 0.5 to 0.62 for various commercial phones (*Figure 5*): these numbers are critical because they translate directly into allowable internal power generation levels. By encouraging the phone manufacturers to increase the CTS to higher levels – our simulations suggest 0.8 – it is possible to achieve better balance between performance and cost.

WHY IS THE CTS IMPORTANT?

The increased CTS leads to better heat transfer and reduced peak temperature at the phone surface. As the internal spreading improves (CTS from 0.43 to 0.84), the device skin temperatures drop below the critical values (no hot spot) and a smaller temperature gradient occurs across the device surface/s (*Figure 6*). The high CTS device dissipates an extra 1.2W before it violates the skin limits compared to the design with low spreading efficiency (CTS = 0.43). For the specific device tested/simulated: every 1°C skin temperature difference leads to 0.16 W change in power, and is achieved by reducing CTS by 0.03.

HOW CAN WE IMPROVE THE CTS?

To enhance the mobile device heat spreading (CTS): a) Optimize the PCB ground plane; b) Use larger copper content for solid ground plane layer; c) Connect all ground pins of key ICs directly to this layer; d) Separate hottest ICs; d) No high Power ICs overlap on opposite PCB sides; e) Place connectors on opposite sides of key ICs where possible.

ALTERNATIVE CTS FORMULATIONS?

The authors evaluated alternative CTS formulations: a) Tavg/T_max; b) Tmax/T_ideal; c) T_ideal/Tmax; d) T_ideal_system/T_real_system. Due to the lack of a physical meaning or independence on ambient Temperatures, it was decided to select the most appropriate version, as defined by *Equation (1)*.

CONCLUDING REMARKS

This article proposes a new, dimensionless thermal spreading effectiveness metric for mobile devices, named CTS (Coefficient of Thermal Spreading). The CTS value quantifies the internal thermal spreading of mobile devices, and is a specific metric to improve the thermal design. It indicates how much a given mobile device can be improved for the given shape/size/form factor. As shown by simulations, optimally designed phones could reach CTS values between 0.8 and 0.9, while poorly balanced phones have CTS values below 0.5. Different mobile devices have different CTS values depending on overall size and internal design. CTS metric is used to help improve the thermal spreading over the device surface and reduce the skin maximum temperature. If adopted by the industry, the CTS Figure of Merit will lead to more thermally balanced phones/mobile devices.

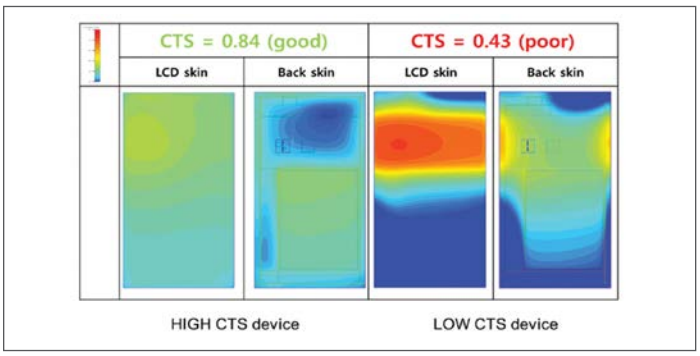


Figure 6. Comparison of calculated CTS values for poorly designed (CTS = 0.43) versus well designed (CTS = 0.84) devices: hot spot evident on poorly designed vs well spread heat on well designed phone skins. Note: CTS calculated using Equation (1) with average/peak skin temperatures from simulations. The temperature scale is the same.

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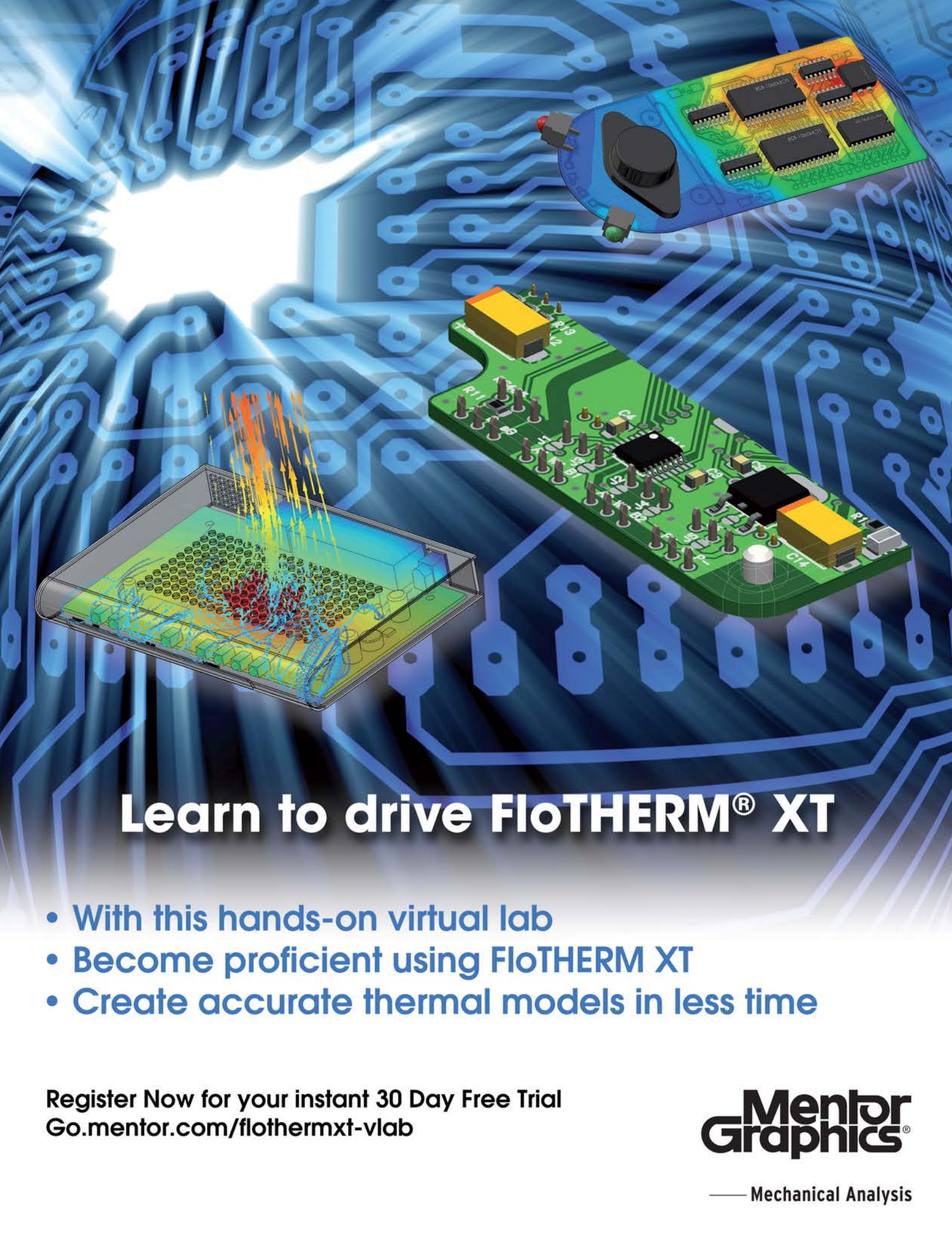
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Keeping Moore's Law Alive

Peter E. Raad
Southern Methodist University and TMX Scientific, Inc., Dallas, Texas

A recent news item[1] described the intended efforts of researchers from IBM, EPFL, and ETH to "keep Moore's Law for another 15 years." Doing so, the article adds, "will require a change from mere transistor scaling to novel packaging architectures such as so-called 3D integration, the vertical integration of chips." The four-year collaborative project called CMOSAIC will investigate cooling techniques that can support a 3D architecture, including "the use of hair-thin, liquid cooling microchannels measuring only 50 microns in diameter between the active chips." The researchers from industry and academia will undoubtedly use myriads of experimental and computational methods to devise their approaches, design their solutions, construct their prototypes, and ultimately test the merits of their hypotheses. This is consistent with what we have always done! However, the inevitability of three-dimensionality in integrated circuits[2] raises an interesting question: how will we know what's happening inside? Whether it is physicians diagnosing and mapping optimal routes for successful surgery or authorities interested in the activities of a suspect operating within the inner confines of a large structure, the problem is the same: how to assess what we cannot access.

Engineers and scientists have long relied on measurements to diagnose system behavior, enlighten thinking, and guide next steps. The dramatic advances in computing machines have made it possible to add numerical simulation as a powerful contributor in our arsenal of investigatory tools for complex systems. Traditionally, though, an individual researcher's strength would favor one approach over another. More recently as computers have become more potent and software packages have become more accessible, experimentation has become in the minds of some only necessary in so far as it provides validation to numerical models. But the community knows too well the dangers of single-minded approaches to any significant problem at hand. The question is then not whether we need to leverage as many individual approaches as possible — analytical, experimental, and computational — but rather which ones are most appropriate to solve our particular problem at hand, which is to figure out the thermal behavior of buried electronic devices and features of interest. This is not an idle question on the semiconductor roadmap. Without a view into the inner workings of complex devices, we will be blind to the actual performance of our designs, and hence condemned to spending our valuable time and energy on trial-and-error rather than rapid prototyping and iterative refinement.

Let us first consider experimentation as it pertains to this discussion. A measurement has the most important advantage of capturing the actual thermal behavior with all the physics as well as the geometric and material complexities that are influencing the operation of a real device. However, the Zeroth Law of Thermodynamics confines us to having to measure temperature indirectly by calibrating the response of a third body to differing temperature levels. There are a number of useful approaches[3, 4], which can be categorized based on the relationship between the measuring implement and what is being measured. We may speak of invasive and non-invasive, contact and non-contact approaches, and within these, we can refer to methods that rely on material behavior (e.g., mercury thermometer, liquid crystal paint), electrical response (e.g., thermocouples, thermistors), optical signature or interference (e.g., infrared, thermoreflectance), to name but a few. Different methods have different strengths, limitations, and figures of merit, e.g., accuracy, resolution (spatial, temporal, and temperature), and precision. Irrespectively, for an implement to record the temperature of a material, the two have to be communicant either physically or optically. Physical contact presents the difficulty of isolating the effect of contact itself, whereas an optical approach limits access to surface or near-surface regions. Given the above, one can now certainly appreciate the challenges of measuring vertically integrated electronic devices, and without even yet considering the additional difficulties presented by the ranges of scales from nanometers to centimeters that are inherent in modern complex devices. Access is a limiting factor.

Computational approaches, on the other hand, do not have issues of physical or optical access. Given a choice of spatial discretization (e.g., finite element/volume/difference) and temporal discretization (e.g., explicit, implicit, trapezoidal), an analyst can construct the computational domain of interest, select the heat transfer physics in play, prescribe initial and boundary conditions, and then wait for the numerical simulation to complete. Of course, (i) different numerical approaches have differing levels of accuracy, stability, and convergence; (ii) numerical simulations cannot represent physics that are not included in the formulation; and (iii) geometric and material complexities can make grid generation quite challenging. The power of computations is that, given an accurate and appropriately convergent solution, we can easily extract the thermal behavior of important features wherever they may be within the computational domain. However, even the most precise and accurate numerical simulations cannot give us results that exceed the fidelity of the input data, be they those associated with the geometry, the material properties, or the heat sources. This is an important point. Numerical simulations can give us gloriously colorful representations of thermal behavior, but only as it pertains to the idealized representation of the device as described by the input data. The numerical results do not automatically comprehend the effects of data uncertainty, natural device aging, or rapid deterioration due to device malfunction. Input data are a limiting factor.

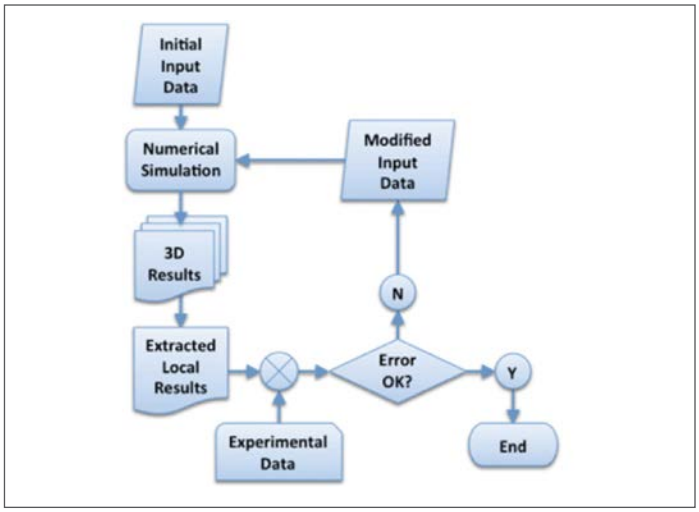

Figure 1. Iterative cycle to optimize input data subject to agreement with experimental data.

So, on the one hand, experiments can comprehend physics and device complexity, but are restricted to specific locations, and on the other, numerical simulations can provide detailed, transient, 3D behavior, but only insofar as the input data represent the actual device of interest. What if we didn't have to pick sides? What if we could marry the two approaches to overcome their respective limitations? Consider the notion of what we might call "tuning approaches" that leverage experimental data to guide simulation. This concept is not unique to thermal analysis of semiconductor devices. In a slightly different approach, perhaps better termed "data assimilation," meteorologists begin by predicting the path of a hurricane starting with a reasonable input data set, but continually modify the progress of the simulation as actual data become available. For our problem at hand, one could imagine simulating a vertically integrated device with the best possible available input data, but then comparing the results in those locations and areas where physical measurements are available in order to generate a more representative input data set. Such an iterative process (*Fig. 1*) would continue until computations and measurements agree to within an acceptable error[5].

There are two important issues to consider: uniqueness and feasibility. First, when solving partial differential equations, particularly if they are nonlinear, it is possible, even probable to have multiple scenarios yield the same temperature value at some given point. Just because the computational and experimental results agree at one point does not make the solution unique. From an information entropy point of view, however, as the number of points involved in the comparison increases, the probability of uniqueness increases considerably. Indeed, as the number of reference points increases into the hundreds and thousands, the probability of two different well-posed problems producing matching results at all those points becomes infinitely small. Secondly, in order for such an iterative approach to be practical, the numerical simulation has to be very fast. The computational time depends on the chosen resolutions in space and in time as well as on the efficiency of the numerical algorithms used to solve the resulting systems of equations. Setting aside algorithmic efficiency and computer speed, the overall time budget is primarily driven by grid size and time step. A difficulty particular to the thermal modeling of integrated circuits is the range of spatial and temporal scales that must be resolved in order for the simulation to be useful. If the smallest grid size were chosen to be larger than the smallest heat source, the effect of the latter would be lost. If, on the other hand, the smallest geometric and thermal features are appropriately resolved, the problem size can become prohibitively large, making multiple solutions within an optimization approach impractical.

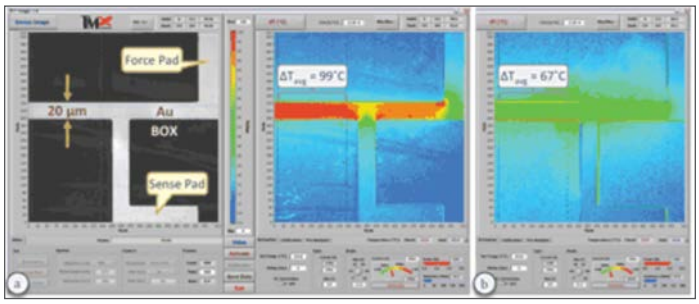

Figure 2. Temperature rise maps over right end of a gold microresistor deposited on (a) silicon oxide and (b) aluminum oxide. The base reference temperature is 23°C. Only the thermal image is shown in (b) since the device image is identical. Images obtained with T°Imager™, a thermoreflectance-based microscopy system (TMX Scientific) (13).

Compact models[6] and ultra-fast numerical approaches[7] have been introduced to reduce computational time by orders of magnitude. Analysts who have at their disposal ultra-fast simulation capabilities become more likely to practice iterative refinement and even experi-

mentally-guided optimization. Additionally, this opens up the interesting possibility of integrating sensors that not only measure locally but also predict thermal behavior in other regions of interest. So then even beyond design and prototyping, highly optimized thermal simulation codes could be embedded within small chips to continually predict internal thermal behavior within operating devices and provide feedback to alter their behavior.

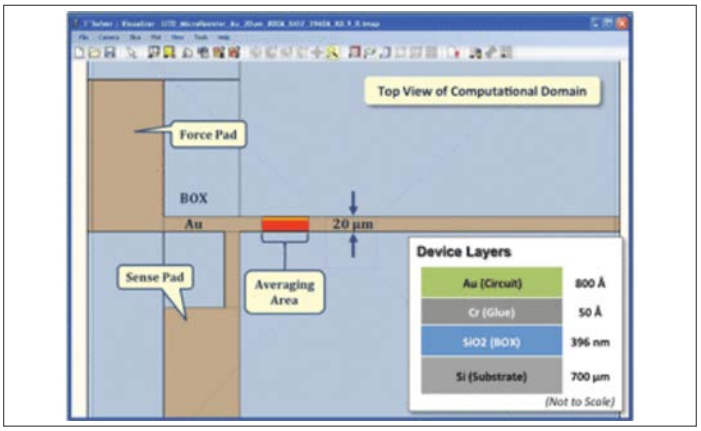

Figure 3. Top view of computational domain showing the area where the temperature is averaged for comparison with experimental results. Inset schematic shows the material composition and height of the layers that make up the microresistor device.

Let's demonstrate the overall idea with an example. Many commercial and academic laboratories are heavily engaged in the search for new buried oxide materials (BOX) at the semiconductor fabrication level and thermal interface materials (TIM) at the die assembly level. Identifying winning candidates and characterizing their actual, in situ thermal impact is a significant and worthwhile pursuit. Several useful approaches exist for measuring the thermal conductivity (or diffusivity) of materials, e.g., 3-ω[8], flash[9], transient thermoreflectance[10], etc.

Thin films present a special challenge for most techniques as does the identification of the contributions of the thermal interfaces, which are invariably process dependent and thus not amenable to generalization[11]. So an interesting example here might be to combine the powers of measurements and computations to extract the actual, effective thermal conductivity of BOX materials. Gold microresistors have been deposited on various metal oxides[12], two of which will be used in this example: Silicon (SiO2) and Aluminum (Al2O3) oxides. Keeping all other conditions identical, we measure the temperature maps with a thermoreflectance-based thermal microscope[5, 13] of the two microresistors (*Fig. 2*) and calculate an average temperature over a section of each of them.

The calculated average temperatures from the SiO2 and Al2O3 devices are 134˚C and 98˚C, respectively. This difference indicates that Al2O3 is a better thermal conductor than SiO2, but does not give us the value of the thermal conductivity of either material. And so we switch to the computational approach, construct a model of, say, the silicon oxide device, and compute with a guessed initial value of the effective conductivity (or diffusivity) of SiO2 (*Fig. 3*). It would make sense to start with the published value of 1.4 W/m-K and even assume that our material interfaces are perfect. Simulating the conduction heat transfer problem with an ultra-fast, self-adaptive computational engine[7, 13] and calculating an average value over the corresponding area that we measured gives an average surface temperature of 102˚C. This discrepancy of 32˚C (or 24%) guides us to modify our input value downwardly from 1.4 W/m-K. Repeating the simulation with effective thermal conductivities for the SiO2 layer of 1.2, 0.9, and 0.8 W/m-K yields average temperature values of 110˚C (18% lower), 128˚C (5% lower), and 137˚C (2% higher), respectively.

A final effective conductivity of 0.83 W/m-K yields the experimentally obtained average temperature of 134˚C. The deduced value for the effective thermal conductivity of thermally grown silicon oxide coincides well with previous measurements obtained with a purely experimental technique[14]. Each of these converged transient computations required just 23 seconds of CPU time on a 3 GHz Pentium 4 desktop computer. Of course, the reader is immediately aware that this approach can be automated and that other important geometric and physical parameters can be included in the optimization process. The purpose of this basic example was simply to step through the optimization process and to demonstrate the power and usefulness of coupling experimental and computational approaches.

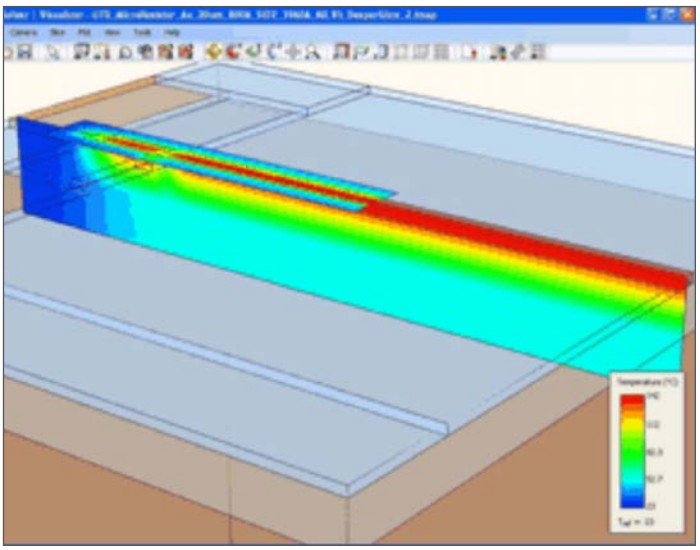

Figure 4. Temperature contours on a horizontal slide on the top surface and a vertical slice through the middle of the microresistor. Computations and images obtained with T°Solver™, an ultra-fast, self-adaptive heat transfer simulation engine (TMX Scientific) (13)

We must remain open to and work toward breakthroughs in metrology. A groundbreaking non-invasive technology, such as what happened with CT-Scan or MRI for seeing within the human body, could come along to enable us to measure temperatures deep within 3D devices. But in the meantime, we need to try to fully leverage what we already have. Extending the life of Moore's Law is a good enough reason.

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Product	Thickness	Thermal Conductivity (Z-Axis), W/mK	Thermal Impedance, C-cm2/W	Tg, C	CTE (Z-Axis), ppm/C		Dk, 1MHz	Df, 1MHz	Breakdown Voltage, kVAC	Flammability
					<Tg	>Tg				
92ML	8mils	2.0	0.52	160	22	175	5.2	0.013	>50	HF V-0

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92ML™ StaCool™ Thermally Enhanced PCB Materials Manage Heat in Power Electronics Applications

Scott D. Kennedy
Senior Product Manager Rogers Corp

Power Electronics Design Trends

Power electronics and associated thermal design is an essential early stage of many product development efforts, especially with growing demand for vehicular and industrial applications. Current trends to increase vehicular driver assistance features, reduce the carbon footprint of vehicles, implement vehicle electrification, and incorporate light-emitting-diode (LED) lighting in automotive and industrial applications all contribute to the growing importance of power electronics.

Electric vehicles require effective thermal management solutions in their powertrain control units. These units include DC/DC converters for either engine management or transmission control. Electric vehicles also feature chassis control units for such functions as electronic power steering. These electric vehicle subsystems operate at high power levels and generate heat that must be dissipated effectively, but without adding excessive weight and volume to the vehicle.

Vehicular lighting is also making a technological transition requiring effective thermal management solutions. Compared to their incandescent predecessors, LED headlights provide improved visibility and enhanced driver safety. But this added performance is not without a price: more than 60% of electrical power supplied to an LED headlight is converted to heat. If heat is not removed from the LED junctions, the elevated temperatures can compromise LED performance and reliability.

The widespread acceptance of this newer headlight technology is expected to drive the growth of the vehicular LED lighting market in the coming years. For example, 100% of the D, E, F-segment cars (luxury and premium vehicles) and 60% of the B, C-segment cars (medium quality vehicles) are expected to have LED headlamps by 2022. Figure 1 highlights the trends of the lighting market from 2007 and expected through 2025.

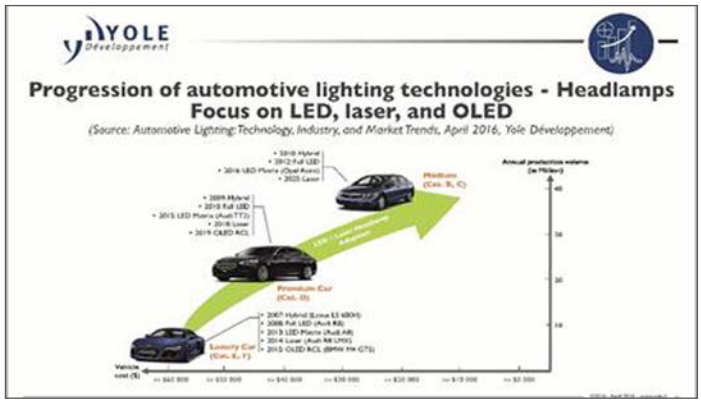

Figure 1. Expected progression of automotive lighting technologies from 2007 through 2025. (Yole Developpement, 2016)

Thermal management is also important for mobile electronics products. The current trend of smaller mobile/handheld electronic devices with increased processing power has resulted in circuits with higher-power-density microprocessors and other semiconductors with thermal management challenges. Figure 2 is a representation of thermal images and external temperatures for a number of different smart phones.

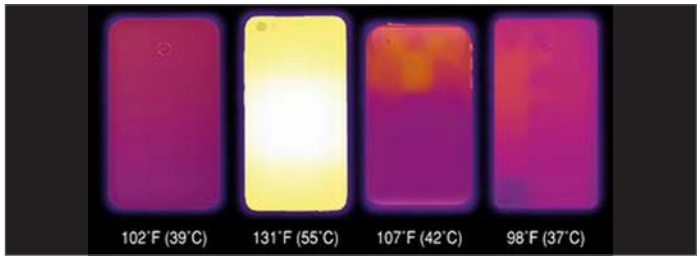

Figure 2. Image showing external temperatures of various smart phone devices.

The increased power densities of modern mobile devices has caused

circuit designers to reconsider their choices of circuit substrate materials, since those materials must now play a greater role in a mobile device's thermal management. The upper operating-temperature limit of most circuit substrates is about 100°C above room temperature (+25°C) or at about +125°C. Traditionally, heat sinks have helped dissipate heat in mobile devices. However, with competitive pricing pressures and the trend for miniaturization, a heat sink may no longer represent a practical thermal solution in a mobile electronic device. Cooling by either external convection air cooling or the use of heat pipe technology is an alternative thermal management approach, but both of these techniques require an additional secondary system adding weight and cost to the final design. They also introduce potential hurdles of quality and reliability that may need to be overcome. Figure 3 below represents a traditional post-attached heat sink approach.

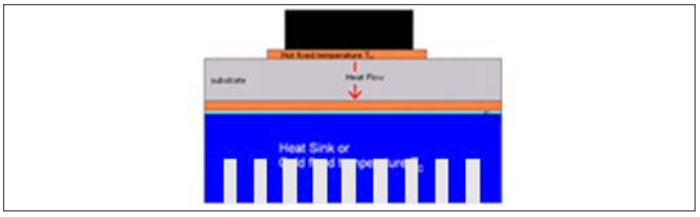

Figure 3. Schematic of a power device mounted on a traditional post-attached machined aluminum or copper heat sink.

Thermally enhanced printed circuit boards (PCBs) like 92ML™ Series and 92ML™ StaCool™ Series materials represent a practical, cost-effective thermal management solution for electronic circuit designs that must minimize weight and volume. Such PCBs can be used in multilayer circuits in place of traditional FR-4 circuit laminates and prepreg materials. The circuit footprint remains small and effective thermal management is achieved without the addition of bulky heat sinks or other heat removal approaches. Figures 4 and 5 describe prepregs and laminates for thermally enhanced PCBs.

Figure 4. Depiction of 92ML™ Series thermally enhanced prepreg.

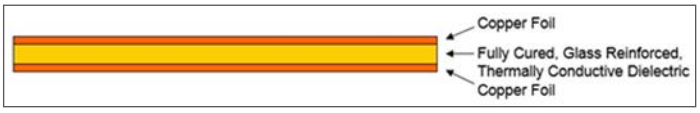

Figure 5. Depiction of 92ML™ Series thermally enhanced copper clad laminate.

Metal-core printed circuit board materials (MCPCBs) or insulated metal substrates (IMS) like 92ML™ StaCool™ materials offer cost-effective, space-efficient solutions for thermal management in modern power modules. They eliminate the need for large, pre-machined heat sinks, thermal pads, thermal greases, springs, wave soldering, and the manual labor associated with the assembly of the traditional power modules (Fig. 6).

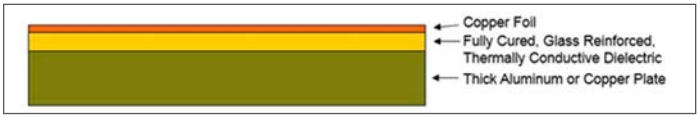

Figure 6a. Depiction of 92ML™ StaCool™ Series thermally enhanced MCPCB or IMS.

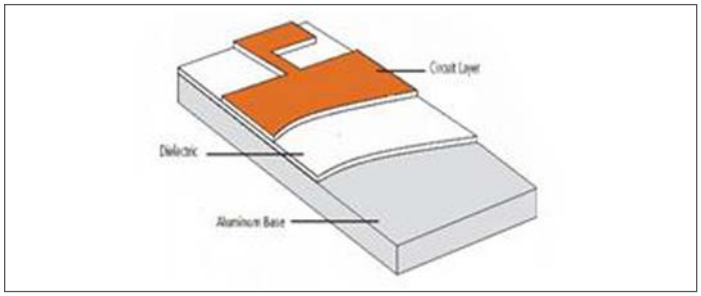

Figure 6b. Depiction of an IMS circuit cutaway view.

The presence of the heat sink is a necessity in order to remove excessive heat from the module. Figure 7 below highlights the importance of a heat sink in assisting the thermal dissipation.

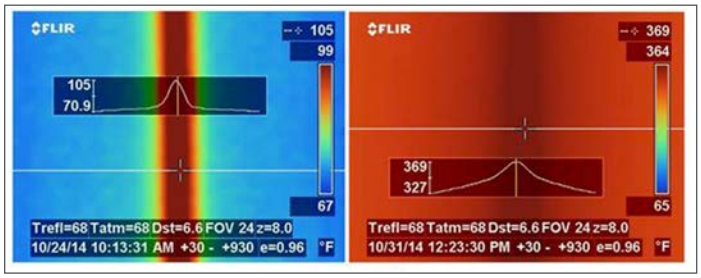

Figure 7. Circuit heating experiment showing the effects of operating with (left) and without (right) a heat sink. Circuit was a 10mil thick RO4350B™ laminate with a bonded aluminum heat sink operating at 85W and 3.3GHz. (John Coonrod, 2015)

Design Advantages of Thermally Enhanced PCB Materials

PCB-based thermal management solutions provide many benefits for designers, including design advantages, decreased labor requirements, improved product quality, and lower capital costs. Compared to traditional ceramic modules, the PCB material approach has the following advantages:

- The use of PCB materials instead of ceramic or other active cooling techniques allows for the use of environmentally friendly materials that are compliant with the end customer and/or local legislative requirements.
- Since dielectric materials are lower in density than ceramic material, the PCB approach reduces vehicle weight for lower CO_2.
- Use of established PCB technology permits large economies of scale.
- Since ceramic modules are limited in the area of embedded devices, the PCB approach allows for integrated designs which incorporate processors and/or power devices within the PCB itself. This is useful for minimizing circuit board heights in tight spaces.

The integration of the heat sink within the PCB material eliminates the need to attach a heat sink separately in the module production process. This eliminates the need for thermal pads, greases, springs, clamps, heat sink assembly, and wave soldering of components. It also allows for the use of press fit connections rather than manually inserted and wave soldered connectors. This greatly simplifies the assembly process as shown in Figures 8a and 8b *(figures on next page)*.

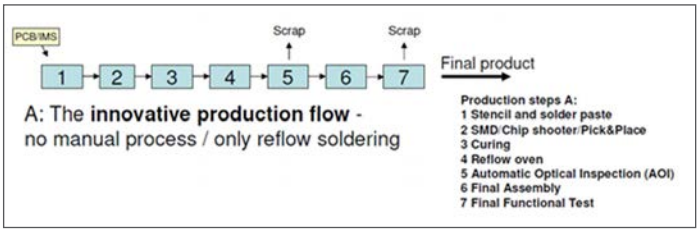

Figure 8a. Stepwise description of the IMS based production process flow for module assembly.

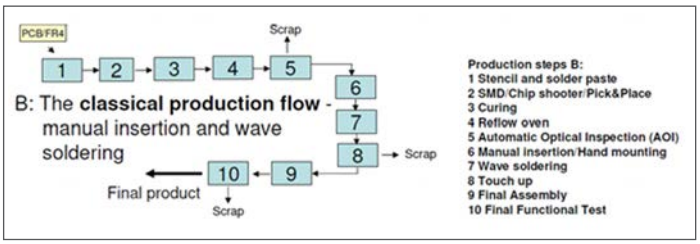

Figure 8b. Stepwise description of the traditional post-attached heat sink production process flow for module assembly.

As illustrated in detailed process steps in Figure 8a, the IMS approach offers the following advantages over a standard post-attached heat sink:

- Eliminates need for module preassembly.
- Eliminates need for manual insertion of surface-mount components, resulting in lower rework or touch-up of soldered surface-mount components.
- Allows automated solder reflow and assembly, minimizing the overall cost of labor.
- Reduction of labor costs and processing steps offset any added automated assembly costs.
- Reduction of module components, with fewer opportunities for failure.
- Reduction of operator contact for more consistent product quality.

Key Material Parameters

In selecting a thermally enhanced PCB material for a thermal management application, designers should be aware of some critical material parameters related to temperature:

Thermal Conductivity

Thermal conductivity is a direct measure of a material's ability to conduct heat transfer. It is the most important property of a thermally enhanced PCB dielectric material. Thermal conductivity is a necessary property to maximize when other means of thermal transfer are not available (i.e. copper vias, heat sinks, coins, active cooling, etc).

The thermal heat flow across the thickness of a dielectric material is inversely proportional to thermal resistance as shown in equations 1 and 2 below.

$$Q = \frac{\Delta T}{R} \qquad \text{(Equation 1)}$$

$$R_\theta = \frac{L}{kA} \qquad \text{(Equation 2)}$$

Where Q = heat flow (W), = change in temperature (K), = absolute thermal resistance (K/W), L = thickness (m), A = area (m2), and k = thermal conductivity (W/mK).

The absolute resistance of the thermal heat transfer can be viewed in much of the same way as the resistance to current flow in an electrical circuit. Figures 9a and 9b below show the two most common circuit resistance configurations.

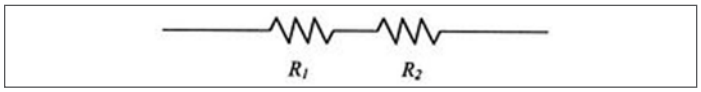

Figure 9a. Series resistance configuration in an electrical circuit.

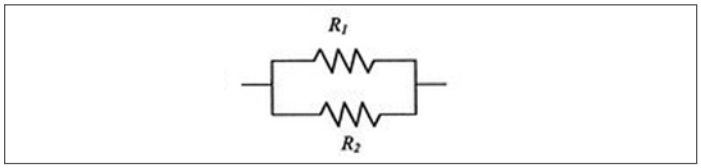

Figure 9b. Parallel resistance configuration in an electrical circuit.

Equations 3 and 4 below highlight the two most common ways to interpret the thermal resistance path across the dielectric material.

$$Series: R_\theta = \sum_1^n R_n \qquad \text{(Equation 3)}$$

$$Parellel: \frac{1}{R_\theta} = \sum_1^n \frac{1}{R_n} \qquad \text{(Equation 4)}$$

Figure 10 highlights the practical application of equations 3 and 4 to actual module construction options.

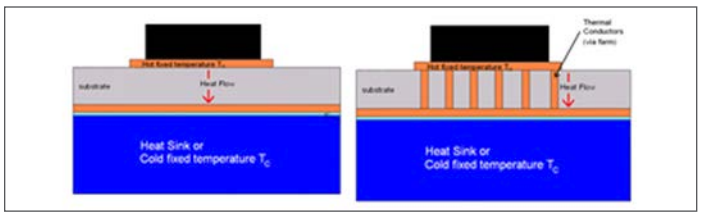

Figure 10. Power electronic module configuration in which a series (left) and parallel (right) configuration thermal resistance path is highlighted.

Standard PCB materials have thermal conductivity values of 1.0 W/m-K or less as measured in the z-axis of the material. Typical FR-4 circuit material has thermal conductivity of 0.3 W/m-K. Thermally enhanced PCB materials have thermal conductivity of 1.5 W/m-k or higher in the z-axis. High-quality thermally enhanced PCB material has in-plane thermal conductivity equal to or greater than the z-axis value, so that heat spreads in the x-y plane of the material as well as through its thickness. This is particularly important when copper plated through holes (PTHs) cannot be placed near a source of heat or when heat dissipation from a module's edges is particularly important. Dielectric material in-plane thermal conductivity of 3.0 W/m-K or higher is considered to be excellent.

Glass Transition Temperature (T_g)

The glass transition temperature, T_g, is a dependable indicator of the thermal stability of a dielectric material. Above T_g polymers have significantly more molecular mobility. This results in a lower modulus and a much greater expansion rate. If the T_g value is too

low, the material will be compromised during exposure to high temperatures, such as during assembly. Lead-free solder attachment typically requires exposure to a temperature of +260°C. If a material softens too early during assembly exposures, there is a risk of blistering, delamination, warpage, or other functional issues. T_g values of +150°C or more are typically required to ensure that the material will survive the necessary thermal exposures.

Coefficient of Thermal Expansion (CTE)

The coefficient of thermal expansion (CTE) describes the expansion rate of a material with temperature. In a PCB, the expansion rate of the dielectric material must be matched to the other materials in the circuit structure otherwise stress will occur at the junctions of different materials, causing board warpage and PTH reliability issues. Ideally, a PCB should have an in-plane CTE value that is between the CTE of copper (17 ppm/°C) and the CTE of aluminum (22 ppm/°C). This will ensure MCPCBs or IMS substrates with optimal coplanarity, with low probability of warpage during assembly and normal operation.

The z-axis or out-of-plane CTE of a PCB material is equally important as the x-y in-plane CTE. Dependable thermoset materials should have z-axis CTE values below T_g that are less than 50-60 ppm/°C. Thermoset materials with z-axis CTE values below T_g that are less than about 30 ppm/°C are considered excellent. Lower z-axis CTE values will result in higher PTH reliability as well as optimal surface component continuity. Figure 11 below shows the impact of T_g on the z-axis CTE.

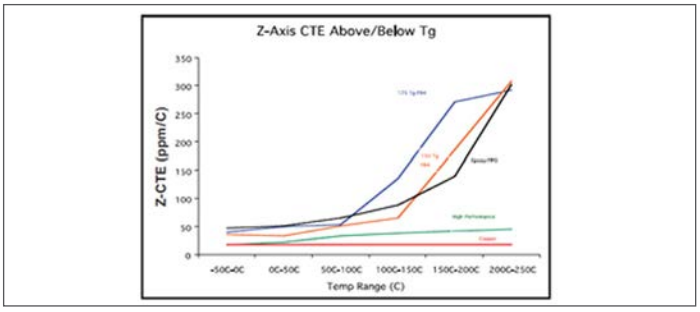

Figure 11. Data from various dielectric materials showing the impact of T_g on z-axis CTE. (A. Aguayo, 2006)

Maximum Operating Temperature (MOT)

The printed circuit material must have the capability to survive for many years at the expected operating temperature of the modules that they will be in. Underwriters Laboratories (UL) has a testing protocol whereby accelerated aging testing is performed that replicates the exposure that the material would see for a testing time of 100,000 hours (or 11.4 years). This MOT test protocol is used to screen circuits for failures such as warpage, blistering, delamination, etc. Good thermoset circuit materials will have an MOT capability of +125°C or more. Excellent materials will have an MOT capability of +140°C or more. The ultimate MOT rating needed is dictated by the end use requirements of the circuit.

Environmental Requirements

PCB materials for consumer application are typically required to have a UL 94 V-0 flammability rating from Underwriters Laboratory (UL). This rating ensures that a dielectric material will self-extinguish within 10 s after exposure to a direct flame. The requirement is application specific and a UL 94 V-0 rating is not required for many applications, such as in space applications.

Circuit materials are at times required to be free of lead-containing components. This lead-free, Restriction of Hazardous Substances (RoHS) condition, also known as Directive 2002/95/EC, originated with the European Union (EU). It restricts the use of six hazardous materials found in electrical and electronic products. All applicable products in the EU market after July 1, 2006 must pass RoHS compliance. RoHS impacts the entire electronics industry and many electrical products as well (RoHS Guide, 2016). This lead-free requirement mostly impacts the solders used with circuit materials. Removal of lead from solder resulted in a need for higher eutectic melting temperatures. As a general rule, the lead-free solder reflow profile is set to a peak temperature of +260°C. Reflow profiles for solders with lead have peak temperatures as low as +225°C.

Circuit materials may also sometimes be required to be free of halogen-containing components. This is an emerging, typically environmentally driven requirement for electronic circuits and mostly found in products for European markets. Few thermoset circuit materials meet the most stringent combination of UL 94 V-0 flammability, RoHS compliance, and halogen-free composition.

In summary, the growth of power electronics applications is fueling a clear need for reliable, thermally enhanced PCB materials to aid in thermal management. Effective thermally enhanced PCB materials like 92ML StaCool Series materials offer many design, labor, cost, and quality advantages over traditional heat-sink power electronic module design approaches. Selecting a thermally enhanced PCB material for a power electronics design is a matter of meeting the requirements of an application, with optimum PCB performance that includes z-axis thermal conductivity of better than 2.0 W/m-K, x-y in-plane thermal conductivity of 3.0 W/m-K, z-axis CTE of less than 50-60 ppm/°C, x-y in-plane CTE between 17 and 22 ppm/°C, and MOT of better than +140°C. Many applications may also require a UL 94 V-0 flammability rating as well as compatibility with RoHS and halogen-free requirements.

Scott Kennedy is Senior Product Manager for Rogers Corp. He has been with the company for 16 years, nine of which were spent in research and development, six in sales, and the past year in his current position. He holds eight US patents and has authored or co-authored four industry articles. Scott holds a BS in Chemical and Materials Engineering and a MS in Polymer Science, both from the University of Connecticut. He also has six years of US Naval submarine nuclear engineering experience.

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SEMI-THERM 33 2017 Exhibits Highlights

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Technical Editor, Electronics Cooling Online

SEMI-THERM 33 concluded last week at Silicon Valley, CA and Electronics Cooling was the only media and content provider present on the exhibit floor. We take this opportunity to thank our readers and contributors who stopped by our booth to learn about our plans for this year including 2017 Thermal Live! We are so pleased to know that many of you like our content, our new webpage, and our emphasis on covering thermal management across multiple disciplines.

SEMI-THERM this year featured many interesting companies showcasing their latest in thermal management solutions –to that extent that I barely managed to attend a couple of technical sessions! Most of my time was spent talking to the solutions providers of thermal management on the exhibit floor. Some of the highlights in the latest product and technology offerings include:

- Continued improvements in Thermal Interface Materials (TIM) –in thermal conductivity, thinner gap-filling and conforming materials.
- Test equipment for characterization of TIMs.
- Excellent advances in higher thermal conductivity materials for enclosures, carriers, substrates and heatsinks –Aluminum with Graphite, Chemical Vapor Deposited (CVD) Diamond, Carbon composites, etc.
- More improvements in user-friendly and better EDA-integrated thermal simulation tools.
- Continued advances in heatsinks –in form factor, materials, fabrication methods and integrated cooling fans.
- Advances in liquid cooling including thermal siphon, better quality and lightweight couplings, no-leak quick disconnects, etc.

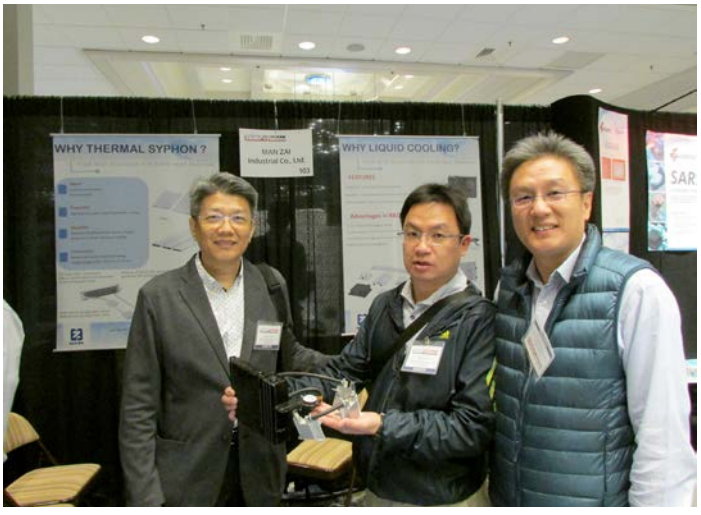
For those of you who did not make it to SEMI-THERM this year, we requested all exhibitors to provide an update on their latest technology and product offerings showcased at SEMI-THERM. In the following paragraphs, you will find brief descriptions of the latest products from thermal management solution providers.

CPC showed its LQ2 Series quick disconnect couplings which it claims have the highest-flow capacity for 1/8-inch connectors in the liquid cooling industry to reduce pressure drops and help optimize liquid cooling system performance. The connectors feature unique elbow and swivel configurations and an integrated thumb latch for easy, one-handed operation in tight spaces like the server racks of large data centers. The color-coded thumb latch is simple and intuitive to operate, contributing to fast, foolproof connections. LQ2 Series also feature a multi-lobed seal for redundant protection against leakage and lasting shape retention during extended periods of connection. The non-spill design allows disconnection under pressure without leaks—a critically important factor in protecting electronics from exposure to fluid and enabling hot swapping of equipment.

Alpha Novatech, Inc. showcased its newly added EZ Clip series of heatsinks at SEMI-THERM33. The traditional Z-Clip has been in use for a long time, and continues to work well. However, installation typically requires slight twisting of the heat sink and/or the use of tools to engage the board anchors. If installed on a fragile device, like a bare die, extra care is required avoid potential damage. The EZ clip utilizes an additional bend section, allowing the operator to grip the clip and easily install without the need for any tools. Only the clip arm needs to move to engage the board anchors, not the heatsink. Installation and removal is much simpler and greatly reduces the chance of damage to a device. Initially, Alpha will offer 6 standard EZ clips. If necessary, Alpha can also create custom clips to meet with a customer's board layout requirement. Existing solder/solder-less anchors can be used.

KULR Technology a leading pioneer in carbon fiber cooling technology showcased its suite of products at ST33. Its Thermal Capacitor PCM heat sink solution provides high thermal conductivity at 10 W/m-K, latent heat capacity of 150-200J/g and low density of 0.7g/cm^3. It is used to keep laser module, embedded camera module and portable devices cool during power usage peak time. Its fiber thermal interface material (FTI) requires low contact pressure of 1.0psi, fills a gap range of 0.2-5.0mm with a bulk thermal conductivity of up to 20 W/m.K. It offers a compliant and non sticky interface that can best be used to accommodate bumpy PCB boards and sliding components. Its thermal runaway shield (TRS) product is a passive cooling solution that prevents lithium-ion battery from thermal runaway propagation. It's lightweight, cost effect and can be used with 18650 and 20700 cells.

Longwin showcased photos of its series of test chambers for racks and servers, coolant distributing units (CDU) for water-cooling modules and flow benches with a flexible duct for air-cooling modules. CDUs work for either single-rack or 1-4U water-cooling modules to verify both water pump performance and system resistance; flow benches provides a validated airflow rate on 1-4U air-cooling modules mounted in the width- and height-adjustable duct to validate their thermal performance. All instruments include programmable control and automated data acquisition.



Man Zai Industrial displayed the latest thermal designs at SEMI-THERM 33rd. We have mainly promoted advanced cooling technology - Thermal Syphon. The major benefits of a thermal syphon is that it can carry more power than a general heat pipe and vapor chamber. Therefore, we can use it to solve high-end power products such as IGBT, Telecom, IT and Cloud computing. Man Zai also offers a wide range of thermal modules for CPU, LED, and automotive electronic device while using liquid cooling system. Of course, we can create custom products to meet with any customer's requirement. Also, our thermal team is equipped with state-of-the-art hardware and software, which includes wind tunnel testing, hydraulic testing equipment and simulation test.

Element Six demonstrated the superior thermal conductivity of its CVD Diamond on a block of ice –two disks of same diameter and thickness with one made of Copper whereas the other a CVD Diamond disk. Technologies using CVD Diamond material include thermal management for component such as laser diodes, laser diode arrays, power devices, RF amplifiers, RF resistors, LED's and others. Element Six also manufactures high power laser optics, beam splitters, IR spectroscopy, high energy particle detectors as well as electrochemistry and products for scientific applications.

Suzhow Tianmai Thermal Technology Co., Ltd founded in 2007 is a developer and manufacturer of Thermal Storage/Insulate Material, Thermal Interface Material, Thermal Diffusion Material, Micro Heat Pipe module, and others type of thermal relative products. Tianmai is dedicated to provide high-efficiency, high-quality, and humanized products and services to its clients. Tianmai continues to improve and master its core technologies as its products and services continue to be qualified by millions of applications all over the world.

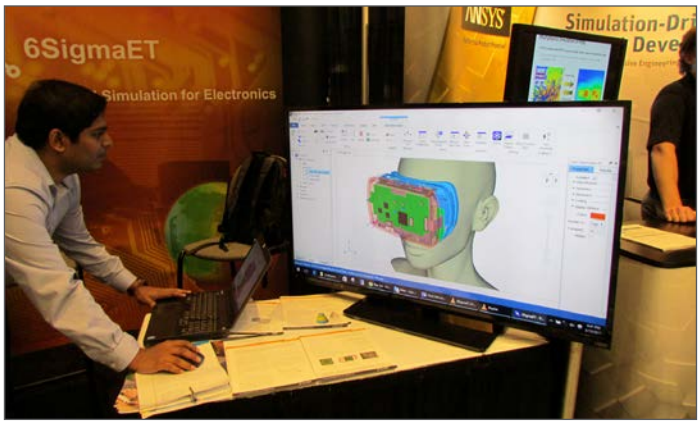
Software Cradle, now a subsidiary of MSC Software demonstrated new features of its HeatDesigner which is specially geared toward thermal management simulation of electronic products. HeatDesigner is structured (Cartesian) mesh thermal fluid analysis software specially designed for electronics cooling thermal analysis. It uses core technology from Software Cradle's scSTREAM general purpose structured mesh thermal-fluid software product.

Jones Tech PLC (USA) showcased its latest thermal gap pad and heat storage material at SEMI-THERM 33. The newly added thermal gap pad from JONES Tech (USA) is capable of 15W/mk and the hardness will be remained at the same range to its 21-830 gap pad (rated at 3W/mk), which is their most popular product currently. Apparently this 15W/mk capable gap pad will be very much desired within the application becoming more compact and powerful in the telecommunication and smart devices markets. JONES Tech (USA) also showcased its heat storage material on display at the show, however the detail information regarding to its application is to be revealed on their website later this month.

QuantaCool showcased its MHPTM passive 2-phase cooling technology, branded as PolarRakTM for data center applications, PolarBoxTM for individual computers, and PolarMaxTM for power electronics. In the photo, Dave Santoleri, QuantaCool's president, demonstrates a PolarBox workstation with simultaneous 2-phase cooling of an over-clocked Intel Core-i7 CPU and an NVidia GeForce GPU. QuantaCool's MHP technology provides superior, cost-effective, and quiet cooling performance. It is safer and more reliable than state-of-the-art liquid-cooled solutions, because it uses no pumps and no water. Coolant circulation is self-regulating, driven by the waste heat and gravity, requiring no external power or controls. Heat can be taken directly from processors and rejected outside the computer room. High performance computers can operate at higher speeds and with more processors without overheating. Data centers can reduce energy consumption, increase capacity, and simplify infrastructure by eliminating indirect cooling steps such chillers, air conditioning, and cooling distribution units. MHP systems are modular and scalable. The components are provided pre-filled with non-hazardous dielectric coolant, and are assembled with drip less quick-connect fittings. The cooling blocks (cold plates) can be installed without special tools. Multiple processors can be cooled via a common condenser; units can be switched-out without shutting down the rest of the system.

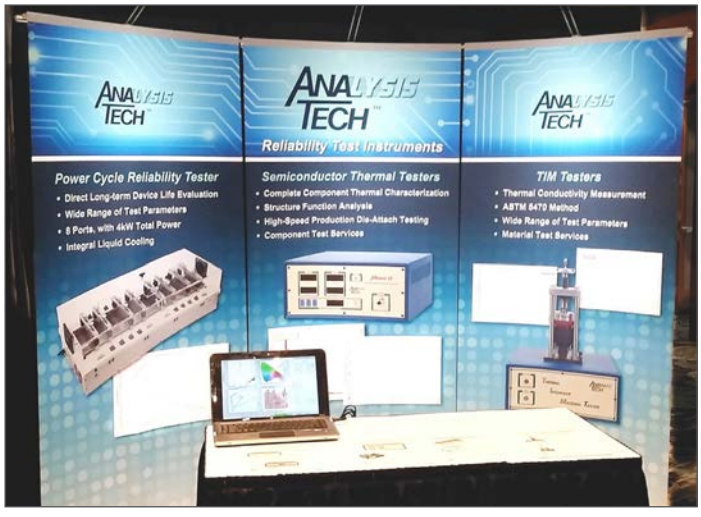
Aavid Thermacore showcased its k-Core® Annealed Pyrolytic Graphite (APG) technology at the 2017 Semi-Therm show. k-Core® is a high-performance advanced solid conduction material system that can help alleviate heat in high power electronics for aerospace, military, and commercial applications. Using solid Annealed Pyrolytic Graphite (APG) material placed within an encapsulate, k-Core® offers effective thermal conductivity of 1000 W/m•K, which is five times greater than that of solid aluminum and three times greater than that of solid copper. k-Core® is also lightweight offering less mass than aluminum. k-Core® can be fabricated by employing most conventional thermal management metals and materials as the encapsulant such as aluminum and copper alloys, ceramics, and composites, depending on the user's need and application. k-Core® key features include: Significantly Reduced Peak Semi-Conductor Temperatures, a higher thermal performance "Drop-In Replacement" for Equivalent Solid Conduction, Smaller Heat Sink Size, Lower Mass than Traditional Aluminum or Copper Heat Sinks, Gravity-Independent (for 0g to >9g environments), Fully Hermetic Encapsulation, Heightened Passive Conductance: In-plane, isotropic room-temperature thermal conductivity up to 1700 W/m•K, can be CTE-matched to Semi-Conductor Materials for Direct Attachment, Rugged, and Resistant to Damage, and Aerospace Qualified.

CEJN Industrial Corporation showed its latest products in quick connect/disconnect coupling for liquid cooling. Fluid products must be leak free, able to quickly connect and disconnect, able to withstand the transferred media and to endure the operating conditions to which they are subjected. CEJN's Fluid products encompass all of these necessities. CEJN's fluid couplers and nipples are available in valved and valve-less designs for low- and medium-pressure applications. Presented at SEMI-THERM are fluid couplings and nipples, hoses and hose kits for fluid applications.



Future Facilities highlighted the eleventh iteration of its leading thermal simulation software, 6SigmaET software for thermal management of electronics. The new edition includes an updated user interface designed for greater speed and accessibility, as well as an increase in the maximum resolution – allowing users to solve models up to 700 million grid cells. In addition to improved gridding capabilities, 6SigmaET has also announced a new Double Precision Solver function, designed to improve the calculation of the temperature residual to solve models in significantly fewer iterations.

The renewed focus on speed and solve time comes following independent research from Thales Global Services, which highlighted that 6SigmaET's meshing time is up to 41x faster than its nearest competitor, with model convergence being reached 2.7x faster in an equivalent design. 6sigmaET has also improved its integration with the Rescale cloud platform. Within Release 11, users can now send models to Rescale for solving, monitor progress and retrieve results directly from the 6SigmaET user interface. They can also now use a client PC to submit and retrieve 6SigmaET jobs from a CFD server on a high-performance-computing cluster in the cloud.



Analysis Tech exhibited its complete product line of semiconductor thermal test equipment for performing device thermal characterizations, transient thermal analysis, and production die-attach and surge testing on any type of semiconductor device. The newly introduced Power Cycler is capable of evaluating power semiconductor device reliability directly with long-term cyclic heating waveforms while continuously monitoring for device degradation. Such testing is quickly becoming essential for power control modules being used in electric cars to wind generators. For material conductivity testing, the Analysis Tech TIM Testers offer precise TIM property measurements, suitable for laboratory or factory workplaces, in a physically robust and easy to use tester. Analysis Tech also offers the CTE Tester for measurement of thermal expansion in electronic packaging materials.

Schunk Hoffmann Carbon Technology showcased two graphite-based solutions for the electronics cooling industry, namely Aluminium Graphite and Latent Heat Carbon, at SEMI-THERM33. Aluminium Graphite combines the low coefficient of thermal expansion, low density, and ready machinability of graphite with the excellent thermal properties of aluminium to create an ideal thermal management material for high-reliability applications. Customized parts, such as base plates or heat spreaders are readily produced with different platings.

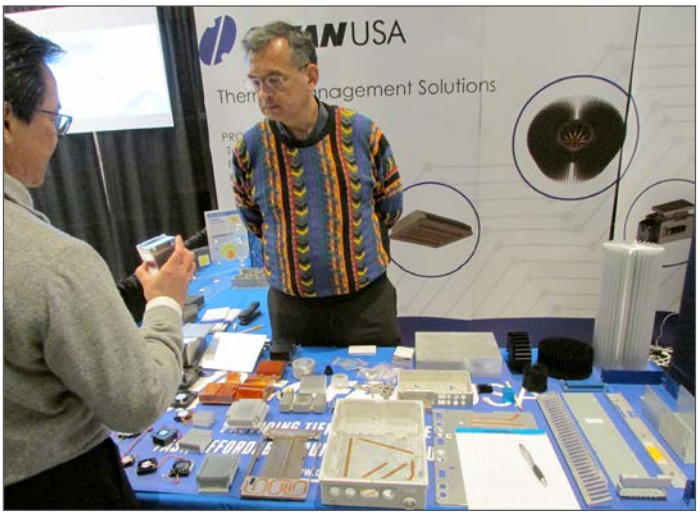
Latent Heat Carbon is a novel approach to latent heat storage units. By using expanded graphite as a preform, a self-encapsulating material with a vastly improved thermal conductivity and low density is produced that enables the rapid buffering of temperature peaks during transient operation. In addition, the patented "Expand to Shape" production process allows for complex, custom designs at attractive cost.

The **NSF** Industry/University Cooperative Research Center for Energy-Smart Electronic Systems (ES2) is collaboration among government, academia and industry to discover and provide industry-driven solutions and technologies to make data centers energy-efficient. ES2's grand vision is to enable cognitive approaches for realizing self-aware and self-managing electronic systems that optimize energy consumption at any specified performance, availability and reliability level. Our mission is to develop the foundations and multidisciplinary solutions to accomplish that vision. ES2 comprises four domestic university sites, one international site and over 20 industry members working on 15 unique research projects.

Fujipoly America Corporation is a world leader in the manufacture of Sarcon® Thermal Interface Materials, which are used to help keep sensitive electronic components cool by eliminating the air gap between the component and heat sink. Fujipoly products range in thermal conductivity from 1.0m W/m-K to 17 W/m-K, offering some of the lowest thermal resistance in the industry. Fujipoly product lineup consists of soft Gap Filler Pads, Conformable Putties, Form-In-Place Gap Fill Materials, as well as custom and standard die-cut thin film materials. Our wide range of material types, coupled with the widest range of thermal conductivity, allows us to meet most design criteria. Fujipoly has nine locations in North America, Europe, and Asia making it easy for us to assist customers at the local level.

Polymatech showed its new industry-leading 50W/m-K thermal Sheet. As customer devices keep shrinking in size while the amount of heat generated is increasing, the higher conductivity sheets play a very important role in electronics thermal management. Polymatech thermal sheets offer a broad selection ranging from commodity-type low cost ones to specialty grades topping thermal conductivity at 50W/m-K. Polymatech also showcased its EMI shielding products, weather-proofing compounds and lower electric resistance and lower compression force connector choices.

Calyos showed off its new evaporator block for higher compute power servers with and with out GPU augmentation. Calyos is a cooling solution provider specializing in the Loop Heat Pipe (LHP) technology. Thanks to its know-how and protected IP, Calyos positions itself as the world leader in LHP manufacturing. Delivering high performing products, Calyos succeeded to address several industries with 2 product lines adapted to different ranges of power. For low power (10W-1000W), the company supplies cooling products for Data Center, Workstation/Desktop and LEDs. For high power (1000W-40KW), Calyos mainly addresses power converter manufacturers (Transports, Wind Turbines, Industrial Processes…).



Cofan USA a 22-company in computer hardware manufacturing industry is a supplier of components, mechanical parts or complete assemblies. Cofan owns factories in China and Taiwan to offers best pricing, fast turnaround, and good quality. Cofan is a high mix low volume manufacturer supplying to telecommunications, electronic manufacturing services (EMS), data center and computer hardware companies. Cofan offers: AC & DC Fans, Heat Sinks, Heatpipes, Metal parts (machined, extruded, forged, stamped, die-cast), Plastics parts (machined, injection molded, pressure molded), Hardware (screws, PEMs, springs) and PCBs and MCPCBs.

KITAGAWA INDUSTRIES America, Inc. is a global leading provider and manufacturer of EMI solution, thermal solution, and shock/vibration management products as well as plastic components. Our thermal solutions include Thermal Interface Materials (TIM) such as silicone and silicone-free pads, phase change gels, ultra-thin thermal films, and dual function materials. Our wide products varieties and custom-layered solutions can be engineered to meet very specific applications requirements. The newest items in our product line include our silicone-free, soft 5W/m*K (CPSH series) and our silicone-free, dual-function absorber and thermal pad (EMPV4 series).

Cooling Source, Inc. is a heatsink manufacturer offering the most comprehensive value-added standardized or custom heatsink solutions for today's global market. Using the very latest technology available to heatsink manufacturers, we offer a wide range of products for our global market clients. Cooling Source' goal is to deliver the highest value to its customers as the premier heatsink manufacturer, offering standard or custom designed products, and services above and beyond what its customers expect. If a customer is unsure whether to use a standard or custom heat sink, allow Cooling Source experts will help to make the right decision for overall cost, tooling time, and delivery time.

AOS Thermal Compounds manufactures the most durable non-silicone thermal interface materials including thermal greases, Sure-Form gap fillers and unique Micro-Faze thermal pads (not phase change material).

Chilldyne Inc showcased its direct-to-chip liquid cooling demonstration system. The Cool-Flo® system offers all the benefits of liquid cooling without reducing uptime and with no worries about leaks. The system utilizes hybrid air-and-liquid-cooled heat sinks and negative pressure to deliver a zero-downtime, leak-proof, low-cost solution. Attendees had the opportunity to participate in the "cut-the-line" product demonstration where they could completely sever a cooling line over an Intel dual xenon server blade without causing any damage to the blade. The system uses negative pressure on both supply and return, therefore if a leak occurs air flows into the system instead of coolant out. The No-Drip/Hot Swap connector which automatically evacuates coolant from a server when disconnected, was also on display. The Chilldyne system is optimized for ease of installation and operation so that all the rack and server level connections do not require a plumber. The system installs into most servers and racks with no modifications making the switch to modern liquid cooling an easy decision.

LISAT is a manufacturer of Thermal Interface Material & EMI products. With HQ in U.S., LISAT has operations in Asia. In U.S., provides Thermal Management Solution to customers & work with R&D Engineers at Design Centres. We provide technical support & samples to our customers to test our materials. LISAT' Asia operations provide manufacturing, converting, technical & sales to customers' worldwide. LISAT products are TIM Pad, Insulator, Silicon Free TIM, Gel, Grease, Mylar, Graphite, Conductive Plastic, Conductive Elastomer, Fabric-Over-Foam, Microwave Absorbing Material, Metal Finger Stock, EMI Shielding Solution, Switching Power Supply, Desktop & Wall Mount Adaptor, Metal Core PCB and Ceramic PCB.

Mentor Graphics Corporation® Mechanical Analysis Division showcased the MicReD® **DynTIM**™ test hardware at SEMI-THERM 33 for accurate, highly repeatable Thermal Interface Material (TIM) testing, and presented the latest release of **FloTHERM® XT**, CAD-centric electronics cooling software. The new DynTIM S standalone solution provides an automated TIM-test environment for rapid bulk thermal conductivity and thermal resistance measurement using thermal transient test technology combined with a sample holder resembling the classical ASTM standard D5470-based methods for enhanced accuracy.

DynTIM S can measure ASTM Type I, II & certain Type III materials covering thermal greases, pastes, phase change materials, gap pads, specific adhesives, certain prepared metallic samples, and more. It features accurate temperature measurement (0.01 °C accuracy), and precise automatic sample thickness control during testing for evaluating bond line thickness (BLT) influence on TIM thermal properties to better characterize insitu performance (Thickness control: 1µ for Type I, 5µ for type II & <10 µ for Type III). DynTIM S is designed for ease of use as a priority, suitable in the laboratory for research and product development, or in quality-testing departments along the supply chain. Combined with **MicReD® T3Ster®** solutions, TIM degradation/aging studies are also possible. For more information, visit : https://www.mentor.com/products/mechanical/

Celsia highlighted several new custom thermal solutions at this year's at SEMI-THERM Symposium. Of particular interest were vapor chamber conduction planes for densely populated electronics, which offer the performance of graphite at a fraction of the cost, UHB (Ultra High Brightness) LED solutions –handing power densities up to 100 w/cm2, and thermosyphons designed for power electronics applications. The company is based in the US with manufacturing at its Taiwan production facilities.

Degree Controls Inc. delivers innovative solutions to thermal issues in a variety of mission-critical applications. Degree Controls make environmental sensors, instruments for system performance testing, and control solutions that deliver precise air flow where and when it is needed most. Degree Controls delivers this at all scales of system infrastructure from miniature sensors for process controls in circuit board environments to comprehensive ventilation and cooling system controls for critical facilities.

ANSYS showed off its ANSYS latest Icepak® and other related tools used in electronic hardware design. If you've ever seen a rocket launch, flown on an airplane, driven a car, used a computer, touched a mobile device, crossed a bridge, or put on wearable technology, chances are you've used a product where ANSYS software played a critical role in its creation. ANSYS is the global leader in engineering simulation. ANSYS helps the world's most innovative companies deliver radically better products to their customers. By offering the best and broadest portfolio of engineering simulation software, ANSYS helps them solve the most complex design challenges and engineer products limited only by imagination.

SUMMARY

In summary, SEMI-THERM showcased newer products, continued improvements in previous generation products, and many new applications. It was heartening to see many new vendors addressing challenges created by many new products in consumer electronics, data center cooling, wearables and networking gear. Electronics Cooling is actively working with thermal management solution providers in the foregoing product segments to bring more coverage in our media products and in SEMI-THERM 2018. To that end, your feedback is very valuable and is appreciated.

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