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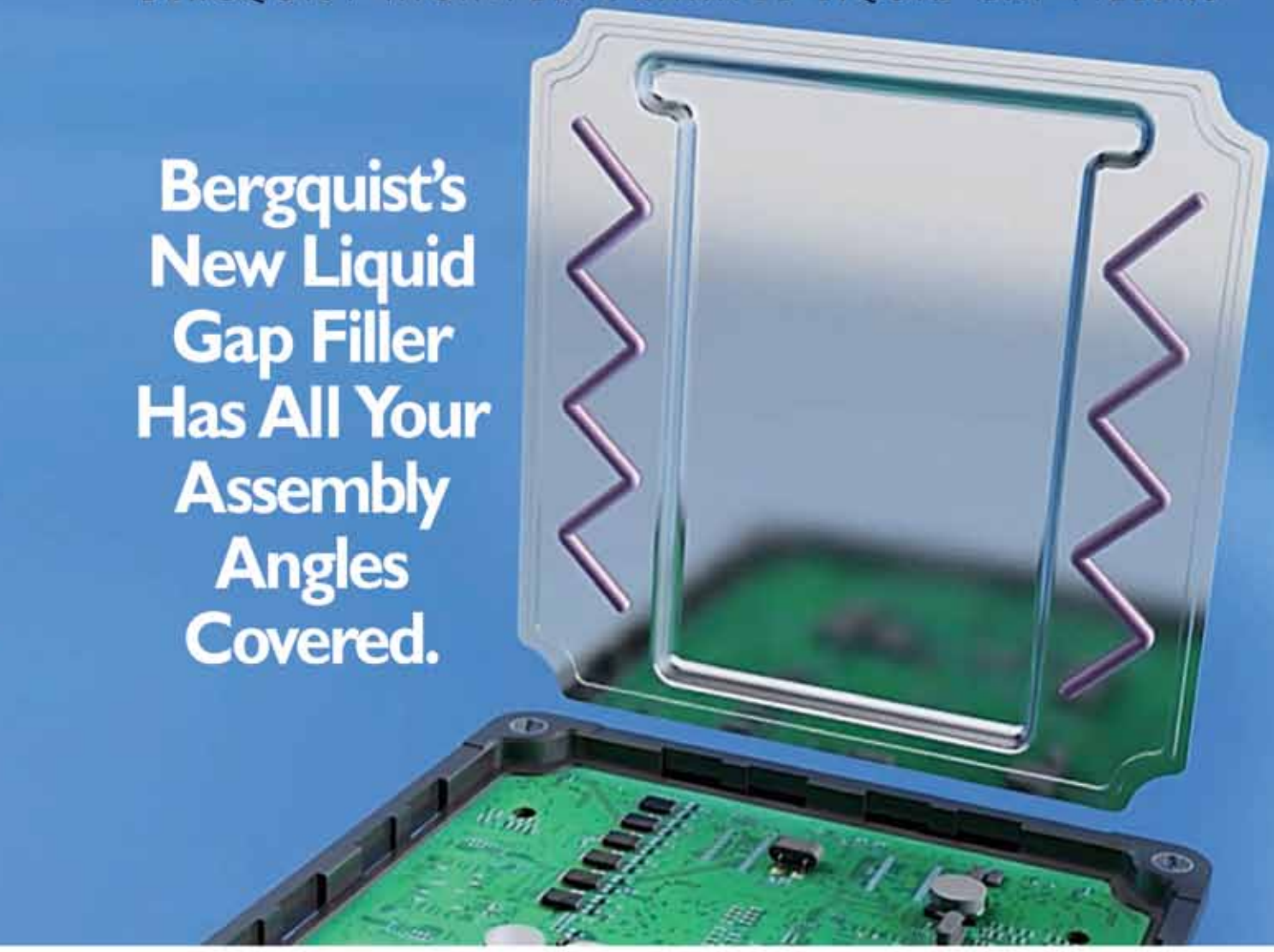

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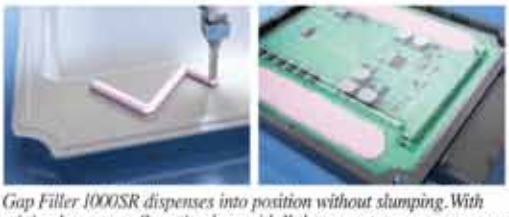

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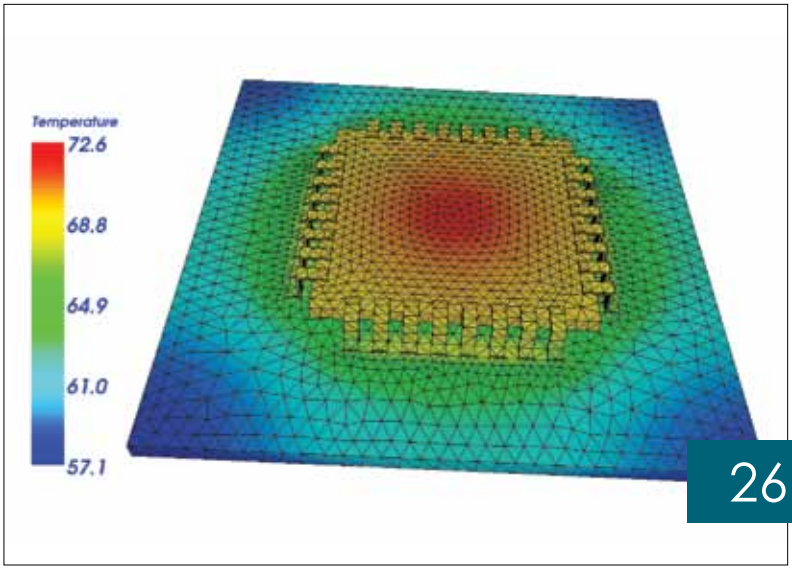

Editorial

Thermal Engineering and the Search for the Higgs Boson

Bruce Guenin, Editor-in-Chief, June 2013

IN SCIENCE, IT'S RARE THAT a revolutionary new theory is not preceded by groundbreaking experiments. More often than not, the timing of such experiments has depended on prior advancements in technology and engineering.

The Large Hadron Collider (LHC) at CERN near Geneva, Switzerland, where the critical experiments to find the Higgs boson were conducted, depended for its success on advances in superconducting magnet technology, with its attendant cryogenic thermal engineering challenges. The LHC produces elementary particles, such as the Higgs boson, as a result of the collision of two beams of protons. In order for the colliding beams of protons to achieve a high enough velocity to be able to liberate the Higgs boson, it is necessary to have stronger magnetic fields than ever before. The scale of implementation of superconducting magnet technology is awe inspiring. The reference below provides a wealth of technical details in this regard.

A key component in the toolkit of the cryogenic engineer is the use of vacuum-insulated vessels to minimize heat transfer from the ambient environment to the liquid helium bath surrounding the magnet. Hence a lot of their efforts are devoted to the design and construction of these enclosures.

In September 2008, a disaster happened during the initial operational tests of the LHC. It occurred when a power supply malfunction led to arcing, which perforated the wall of the vacuum jacket surrounding two magnets and their liquid helium baths. This led to the rupture of these enclosures and rapid release of tonnes of liquid helium with explosive force. This resulted in damage to 50 magnets and their mounting structures. The event necessitated the manufacture and installation of replacement magnets, leading to a delay in the LHC achieving full operational status for a full year.

Normally, for thermal engineers working in more conventional electronics cooling environments, when their design goes awry, the end result is not nearly so dramatic. There may be a cooked chip or PCB. If there is liquid cooling being used, there may be a burst pipe, but nothing on this scale.

However, even our more conventional designs are dependent on the soundness of the engineering of other parts of the total system, for them to perform as intended in the field. For example, a carefully characterized thermal interface material, that was supposed to provide a low-thermal-resistance path from a high-power processor to a heat sink, is dependent on the design of other components and a careful assembly process in order to maintain the required contact force for successful operation over the lifetime of the product.

The story of the mishap at the LHC has a moral for all of us in that we live in a very interdependent world of engineering. It's critical in product development that we fully understand any risks relating to a malfunction in one part of the system precipitating failure in other parts, leading to even more calamitous consequences. We should all do our part to promote cross-discipline discussions to ensure that these risks are fully anticipated and successfully managed.

[Reference: Wikipedia -- http://en.wikipedia.org/wiki/Large_Hadron_Collider]

* * * *

My esteemed colleague and friend, Clemens Lasance, announced his decision to resign from the editorial staff several issues ago. However, he generously stayed on until we remaining editors were able to engage a worthy successor. We have now completed that process.

I'd like to take advantage of this opportunity to thank Clemens for his many contributions to this publication. Over the nearly two decades since the founding of *Electronics Cooling*, he has been its most outspoken face to the public in advocating approaches to thermal engineering that he believes to be the right ones. We will miss his passion and intellect and wish him the best in his future endeavors. We hope to have the pleasure of publishing an occasional piece from him in his new role as emeritus editor.

I'm pleased to announce Dr. Peter Rodgers has now joined us on the editorial staff. Peter has had a distinguished career in thermal engineering. He is currently an associate professor of mechanical engineering at the Petroleum Institute in Abu Dhabi, UAE. He has held prior positions as the University of Limerick, University of Maryland, and Nokia Research. He is an active participant in the major thermal conferences in the US and Europe and has received a number of awards recognizing his contributions to thermal engineering. We look forward to working with Peter to find even better ways of providing you, our readers, with practical technical information and analysis that is of lasting value.

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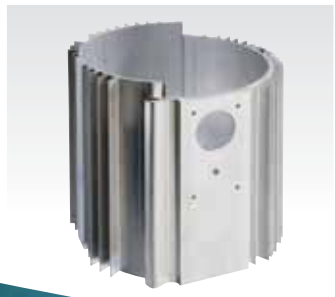

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Cooling Matters

Applications of thermal management technologies

MICROSOFT TO EXPAND HYBRID INDOOR-OUTDOOR 'ROOFLESS' DATA CENTER

Microsoft has announced that the company's newest data center campus will be expanded to include two more data center facilities. Located in Boydton, Va., the facility houses server racks both indoors and outdoors within larger enclosures as part of a hybrid design engineered to reduce operating costs and increase energy efficiency.

The primary concept behind the success of the new hybrid data center is the use of IT-PACs, pre-constructed, container-like modular data centers that are capable of operating in a variety of environments. Engineered with an adiabatic cooling system, the IT-PACs pull fresh air from outside through a layer of "wet media" to cool the server racks inside. According to Microsoft, the system allows the company to keep the servers cool using only 1 percent of the water typically consumed in a traditional data center.

Microsoft's wide development of the IT-PACs was triggered by an experiment completed in 2008, in which the efficiency and condition of a server rack placed in a pup tent outdoors was evaluated over a period of eight months.

Source: Data Center Knowledge

NANOLASER TECHNOLOGY ROOM-TEMP. BREAKTHROUGH MAKES FASTER COMPUTERS

Researchers at Arizona State University have announced a breakthrough in nanolaser technology that could enable electrically-powered nano-scale lasers to perform reliably at room temperature and facilitate their use in a variety of practical applications.

While scientists believe nanolasers have the potential to help computers and other electronic devices operate faster, the large amount of cooling required by the nanolasers makes their use impractical.

According to the ASU research team, in order for nanolasers to be useful in electronic and photonic applications, the laser must be able to operate at room temperature without a refrigeration system; must draw power from a "simple battery" instead of another laser; and able to emit light continuously.

A number of challenges remain, including integrating nanolasers into a photonic system-on-chip platform and increasing the lifetime of laser operation. However, a significant hurdle has been overcome with the success of the team's latest achievement.

Source: AZ State University

SCIENTISTS ANSWER MYSTERY - HOW Bi2Te3 AND GaAS ARE COMBINED

While researchers have long known that thin films of bismuth telluride (Bi2Te3)—which converts heat into electricity or electricity into cooling—can be combined on top of a gallium arsenide (GaAs) foundation to create cooling devices for electronics, a team from North Carolina State University (NCSU) and RTI International have answered the question as to how they are combined for the first time, a breakthrough that could lead to more efficient technologies for powering or cooling electronics.

Scientists have been unable to determine how the two materials are held together because their atomic structures are not compatible, preventing a chemical bond from forming. However, using 'Super-X' x-ray spectroscopy technology in combination with an aberration-corrected scanning transmission electron microscope, the NCSU and RTI researchers were able to determine that the materials were in fact held together by the addition of a thin surface layer of gallium telluride, which is created during the development process, and weak electrical forces known as van der Waals bonds.

Source: RTI International

Datebook

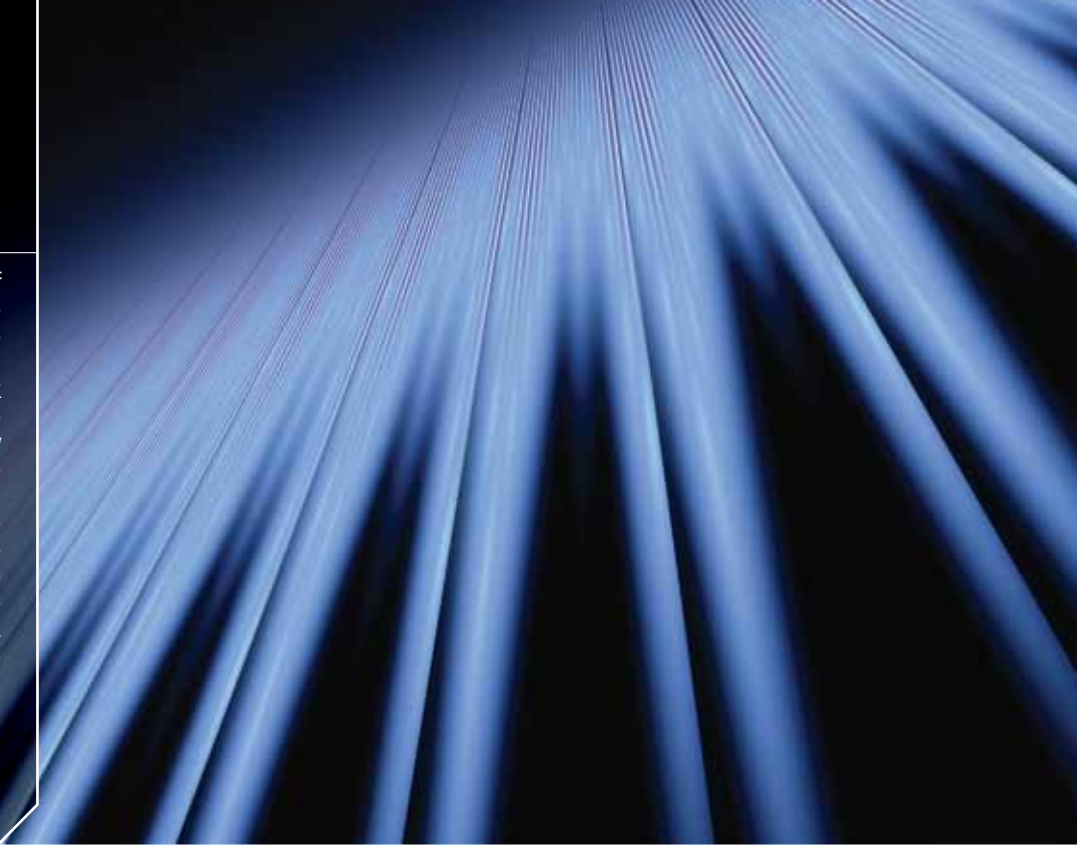
JUNE 6-7, 2013	JUNE 30-JULY 4, 2013	JULY 14-19, 2013	JULY 16-18, 2013
Advancements in Thermal Management 2013 Denver, CO **www.thermalnews.com/conferences**	**The 32nd International Conference on Thermoelectrics** Kobe, Japan **http://ict2013.its.org/taxonomy/term/17**	**ASME 2013 Summer Heat Transfer Conference** Minneapolis, Minn. **www.asmeconferences.org/HT2013/index.cfm**	**InterPACK 2013** Burlingame, Calif. **www.asmeconferences.org/interpack2013**

VIBRATION-FREE COOLING TECHNOLOGY TO REPLACE MECHANICAL COMPRESSORS IN SPACE APPLICATIONS

Researchers at the University of Twente in the Netherlands have developed a new technology for cooling optical detectors on spacecraft that could help the sensors better detect weak "space signals" that originate from far-away, extremely cold sources. The new development is part of a project commissioned by the European Space Agency.

Current cooling systems use mechanical compressors to help optical detectors reach temperatures of just few degrees above absolute zero (-273°C) in order to measure these signals. However, the mechanical compressors can create vibrations that affect the sensitivity and performance of the optical instruments.

Source: The University of Twente



NEW SUPER-COOLING TECHNIQUE BRINGS QUANTUM COMPUTING CLOSER TO REALITY

Scientists at the University of California Los Angeles have developed a new technique for super-cooling molecules by combining two traditional atomic cooling technologies that may prove to be a breakthrough for quantum computing.

According to Eric Hudson, a UCLA assistant professor of physics, scientists have only succeeded in creating a few specific kinds of the ultra-cold molecules needed to transmit and store data in quantum computing during the past decade.

Since it is difficult to theorize which materials—if any of the few currently in existence—might be used in quantum computers or other future applications, the development of a method that could be used to create many different ultra-cold molecules is significant. Hudson and his colleagues were able to prevent most of the barium chloride ions used in the experiment from "vibrating and rotating" by immersing them in an ultra-cold cloud of calcium atoms assembled by laser beams—a magneto-optical trap.

The barium chloride ions were then confined within the cloud with help from "specialized rods with high, oscillating voltages, as part of an ion trap." Halting the movement of the molecules is a necessary step before they can be used to store data because any data a scientist attempted to store in room-temperature molecules would "quickly become gibberish," according to Hudson.

While magneto-optical and ion traps are not considered to be new technologies in the field of molecular physics, Hudson and his colleagues are reportedly the first group to create a cloud of ultra-cold molecules by combining these methods.

"Our technique is a completely different approach to the problem — it is a lot easier to implement than the other techniques and should work with hundreds of different molecules," Hudson said.

Source: The University of California Los Angeles

AUGUST 4-7, 2013	AUGUST 12-15, 2013	AUGUST 14-15, 2013	SEPTEMBER 24-26, 2013
The North American Thermal Analysis Society Annual Conference Bowling Green, Ken. **http://www.natasinfo.org/conferences**	**NASA Thermal Fluids and Analysis Workshop** Kennedy Space Center, Fla. **http://tfaws.nasa.gov**	**The LED Show** Las Vegas, Nev. **www.theledshow.com**	**PCB West 2013** Santa Clara, Calif. **www.pcbwest.com**

A System Perspective for Electronics Cooling

Jim Wilson
Engineering Fellow, Raytheon Company

A **FRIEND OF MINE** who was an aspiring plumber once stated that all you need to know to be a plumber is that you get paid on Friday and that waste flows downhill. Maybe there is a similar analogy for thermal engineers that regardless of when we get paid, thermal energy will flow in the direction of decreasing temperature. The direction of heat flow with respect to temperature gradients makes for an easy fact but it is a fairy tale that electronics cooling systems are always inherently simple. Designers of electronics cooling systems have a wide variety of technologies and hardware to consider and understand. When faced with a challenging design problem a good practice is to research alternative techniques that have advantages, such as the ability to shrink the packaging size or support higher heat flux levels among other factors. Technical papers such as those in this magazine can help the designer understand these technologies and design options. However, the decision to use the more advanced techniques and hardware is often more complicated. I am often asked why our electronics cooling design for a particular product doesn't use xxx where xxx might be two-phase cooling, thin film thermoelectric, or IC microchannels for example. The reason some of these techniques are not widely used isn't because they do not have good thermal characteristics or because we don't have smarter thermal engineers. They just may not be the best choice at the system level.

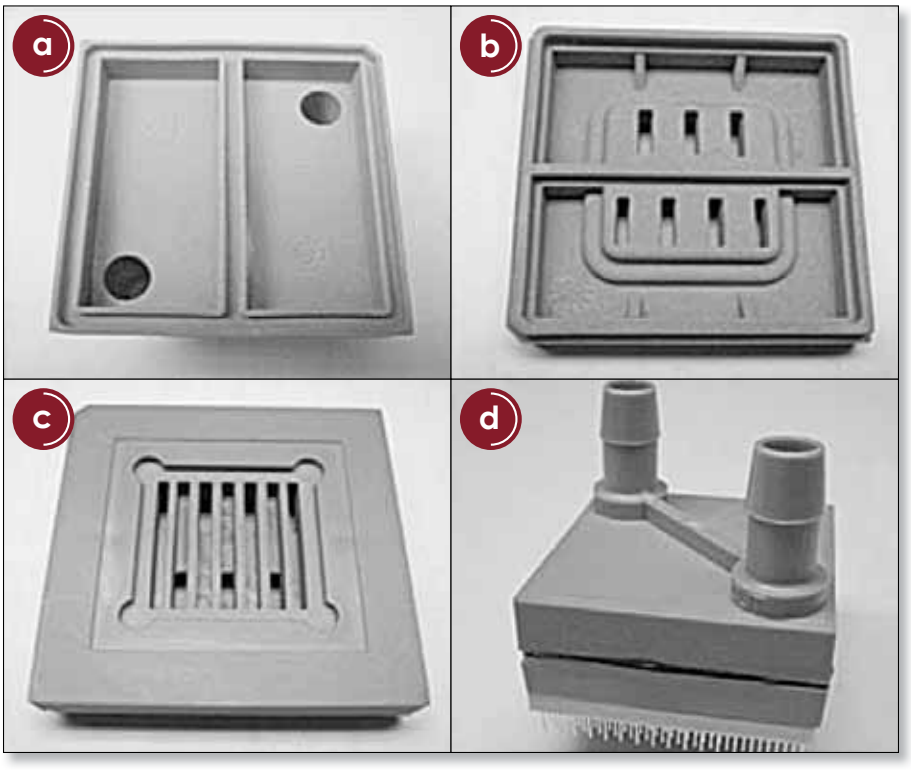


FIGURE 1: Microchannel cooling for an IC [1].

The need to understand the system impact became evident to me when I was trying to use some thin thermoelectric coolers in a design to reduce local temperature gradients on some relatively low powered devices. While the addition of a thermoelectric cooler showed a thermal improvement compared to the original design, we had to allocate volume and interconnects for supplying a separate voltage for the coolers. A more fair comparison was to trade the thermal performance that would exist if this volume was used for thermal management with other approaches such as a high conductivity heat spreader. When examined at this level, the benefits of adding the thermoelectric cooler were minimal.

It is common just to focus on the specific part of the problem you are trying to solve and lose sight of the system level implications. A couple of examples from past issues of *Electronics Cooling* are shown below. I picked them for their pictures and certainly do not wish to imply that these articles are

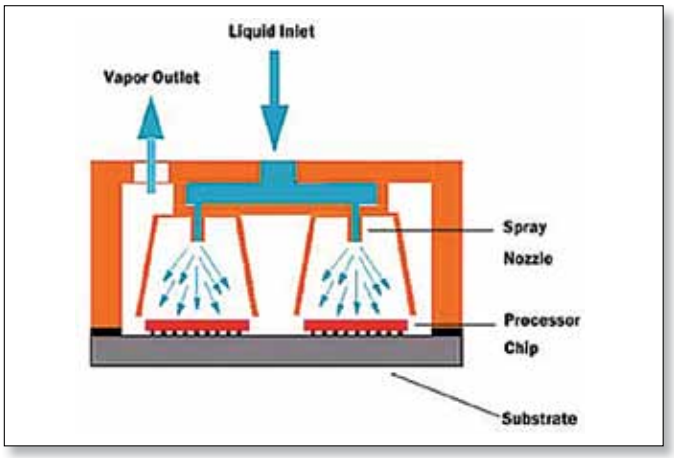


FIGURE 2: Chip level spray cooling [2].

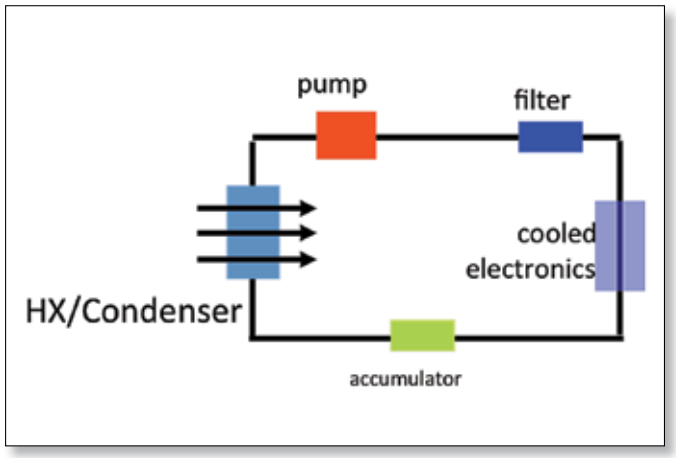


FIGURE 3: Some other components needed for spray cooling.

incomplete. In fact, both of the articles are excellent technical descriptions of the particular issue they describe. Figure 1 is repeated from a nice article on implementing microchannel cooling for a Silicon IC [1] and illustrates the manifolding block and assembled single chip module. While the theme is based around the adjective micro, notice the physical size of the fluid manifolding and interconnect. If the design is only to cool one IC, then accommodating this physical size might be acceptable. However, if this approach was to be used on many ICs, then the complexity of routing the fluid

becomes significant and the fluid distribution system becomes dominant in the packaging density. RF systems often have the packaging density, or chip to chip spacing, dictated by electrical considerations and may not be compatible with the hose and fitting sizes. There is still room for improvement in microfluidic concepts and hardware. It is also worth noting that not all electronics systems have the same packaging density constraints. Generalized conclusions from an application similar to data centers may not be applicable to systems that are more sensitive to weight and volume such as aircraft and portable systems.

A second example is shown in Figure 2 which illustrates a representative spray cooling concept from an overview article on chip cooling techniques beyond air. The system implications of implementing two-phase cooling can be significant. Figure 3 is a simplified diagram of a closed loop cooling system where the cooled electronics are represented by the box on the right side. While some of the other items are obvious, a complete implementation trade must consider filtration, maintenance, the size of the condenser, potential need to restrict orientation, etc. Specifically for two-phase with multiple heat sources, the system trade must also include the complexity of manifolding and controlling the flow to the different heat sources. The answer may still be that the more advanced cooling technique, such as spray cooling, is the right answer, but it is important that the full trade space be examined.

Sometimes the focus on just the chip cooling technology is driven by academic interests that fulfill the need to fully understand the process. Other times this focus can be marketing driven where the benefits of the advanced cooling technique are highlighted but potential complexities of implementing the technologies are minimized because they detract from the intended message. My reminder to the readers is to consider the complete electronics cooling system and the necessary other components that go along with a particular cooling technique.

REFERENCES

[1] Colgan,E., et al, "A Practical Implementation of Silicon Microchannel Coolers", Electronics Cooling, Nov 2007

[2] Simons and Ellsworth, "High Powered Chip Cooling — Air and Beyond", Electronics Cooling, Aug 2005

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Electronic Performance Impact of Elevated Humidity Environments - Implications for Free Air Cooling of Data Centers

Bruce Guenin
Associate Technical Editor

INTRODUCTION

THE COMPUTER industry is exploring various options for reducing the cost and energy consumption associated with cooling data centers. The use of liquid cooling in the data center has long been exploited as a more energy efficient means of heat removal than forced air cooling. However, more recently, there has been considerable interest in cooling data centers by means of circulating outside air through the data center to cool the computer hardware directly and then exhausting it to the outdoors. This achieves energy efficiency by eliminating active refrigeration, for at least part of the year. This cooling method is commonly called "free air cooling."

Recent articles in this publication reflect the increased attention being directed at free air cooling. In the December, 2012, issue, an article described the design, energy efficiency, and bring-up challenges of a predominately free-air-cooled data center in the Pacific Northwest region of the US [1].

In that same issue, a Technical Brief article provided an update of the activities of the ASHRAE Technical Committee 9.9, devoted to datacenter cooling technologies and the development of best practices in that regard [2]. The article described the evolution of the maximum allowable data center temperature from 25˚C in 2004 to the creation of additional environmental classes in 2011 that allow temperatures up to of 40˚C and 45˚C, at maximum values of relative humidity (RH) of 40% and 32%, respectively. However, early experience in the deployment of free air cooled data centers indicates that, under more extreme weather conditions, the RH can reach levels exceeding the dew point [1, 3]. One expects that, over time, the technology will mature to the point that these episodes will occur less frequently. However, one would anticipate that it will always be more difficult to control RH using free air cooling than with the more traditional, and energy intensive, vapor-compression cooled air conditioners. Nonetheless, the expectation of this ASHRAE committee is that, over time, data centers will be migrating to higher temperature and relative humidity conditions than is now customary.

For reasons of economy and ease in manufacture, many of the components currently used in electronics systems employ organic materials. As is well known, organic materials are, in general, permeable to moisture and will, over time, absorb moisture until a concentration level is reached that is in equilibrium with that of the ambient air. The precise value of the moisture concentration will depend on the ambient air temperature and RH and the temperature of the component in

TABLE 1: EQUILIBRIUM MOISTURE CONCENTRATION

Air Temp	Air RH	BT Temp	RH @ BT / Air Interface	Conc @ BT / Air Interface	Ratio: Conc/ Baseline Value*
(˚C)	(˚C)	(˚C)	(%)	(mg/cm^3)	
20	20%	60	2.4%	0.074	0.4
20	40%	60	4.7%	0.20	1.0
20	60%	60	7.1%	0.33	1.7
40	20%	60	7.4%	0.35	1.8
40	40%	60	14.8%	0.83	4.2
40	60%	60	22.2%	1.52	7.7

***NOTE:** Baseline Conc. Value = 0.2 mg/cm^3

question and its material composition.

It has long been known that excessive levels of moisture in organic materials used in electronics can lead to reliability problems. This phenomenon has been studied in particular for materials that are suddenly heated to a high temperature such as during the solder reflow process. So-called "popcorn" cracking is a dramatic and typical failure mode in this situation. More subtle moisture-induced failures can occur once an electronic system is in the field. Examples are those caused by stress resulting from the swelling of polymers due to moisture intrusion or to electrochemical migration in the presence of electrical bias and moisture. These effects have also been widely studied. However, there has been much less study on the effect of moisture on the performance of passive components and active subsystems.

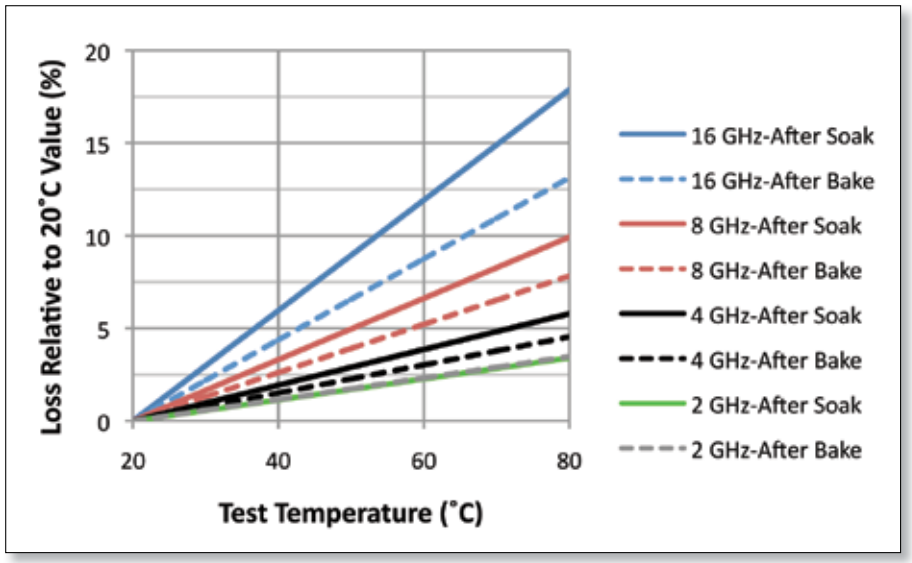

FIGURE 1: Graph of signal loss for a stripline structure versus temperature, frequency, and moisture content resulting from 1) soak process (1.76 mg/cm^3) and 2) bake process (0.30 mg/cm^3).

CASE STUDY ANALYSIS

Moisture Concentration in the Package Laminate Material -- BT

A recent Calculation Corner column was devoted to the calculation methodology for modeling moisture diffusion [4]. It dealt with BT (bismaleimide triazine), a fiber-reinforced polymer commonly used in BGA (Ball Grid Array) packages. The article demonstrated a method for calculating the equilibrium concentration of moisture at values of ambient temperature and RH within and slightly beyond the current ASHRAE limits. Table 1 provides values of saturated moisture concentration in a BT substrate, assumed to be in an operating system, such that its temperature is 60˚C. [Note that, as shown in the article, the elevated temperature of the BT leads to a lower moisture concentration than had it been at ambient temperature.] All of the assumed values of ambient temperature and RH are within the current allowable ASHRAE range except for the 40˚C/60%RH value. Using the concentration at 20˚C/40%RH, namely 0.2 mg/cm^3, as a baseline value, one sees that, at the top end of the allowable range, the moisture concentration is four times that, at 0.8 mg/cm^3. We will return to these values in the discussion in the following section.

Another thing to note in the referenced analysis is that the time for the moisture to reach equilibrium in BT under these ambient conditions is on the order of only a few weeks.

Effect of Moisture Concentration on High-Speed Signal Propagation

A recent study measured the high-speed signal propagation along a copper trace, 21 μm wide and 15 μm thick and 50 mm long in a stripline configuration, typical of what would be used in a package substrate [5]. The trace is sandwiched between two layers of a low-loss, FR-4 type dielectric, each 130 μm thick, 1.4 mm wide and 50 mm long. Each dielectric layer has a copper plane bonded to its outer surface. The signal propagation is measured using a vector network analyzer at frequencies between 2 and 16 GHz at two different moisture concentration levels in the dielectric. Tests were performed at each of the specified frequencies over a range of temperature values from 20 to 80˚C.

The first moisture level was achieved by a "soak" exposure at 30˚C/60%RH for one week. The calculated moisture concentration at the stripline location (along the centerline of the dielectric) is 1.8 mg/cm^3. This value is comparable to that calculated for the BT at the upper end of the range.

After the completion of the first set of tests, the sample was "baked out" and then retested over the same frequency and temperature ranges. The bake out condition was 125˚C for 1 week. The calculated moisture concentration at the stripline location following the bakeout is 0.3 mg/cm^3. This is comparable to the baseline moisture concentration in the preceding case study.

The results are plotted in Figure 1. The graph compares the signal loss (attenuation) at a given temperature minus the loss measured at 20˚C. There are two families of curves plotted, representing the sample in the "after soak" and the "after bake" conditions. We see that the soaked sample shows more signal loss than the baked one. The effect is more pronounced with increasing temperature and frequency. In the worst case reported here, the loss at 16 GHz and 80˚C is 36% greater for the soaked sample, compared to the baked one. In general, at these very high frequencies, the noise margins

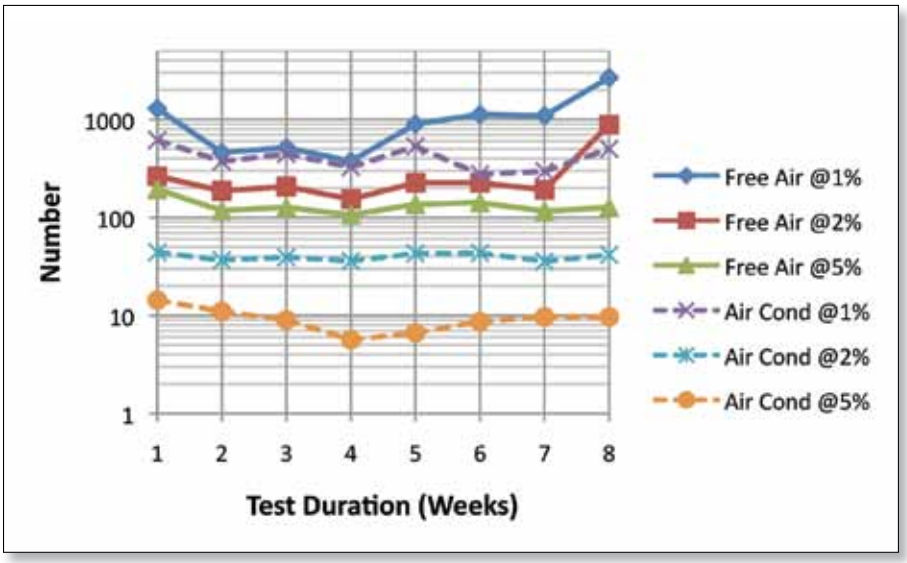

FIGURE 2: Number of data packets per week experiencing indicated levels of dropoff in data throughput (1%, 2%, and 5%).

are tighter. The increased attenuation measured here could potentially lead to increased bit error rates unless it was anticipated in the design phase and effectively accounted for.

Effect of Moisture Exposure on a High-speed Network Switch

Another recent study measured the data throughput of two different populations of three identical network switches over an eight-week period [6]. One was maintained under environmental conditions representative of a benign air conditioned data center environment: 20˚C/50%RH. [Note that these conditions are close to the baseline values in the first case study.]

The second environment was chosen to be representative of conditions experienced in a free-air-cooled environment. It was conducted in an environmental chamber in which the temperature/RH setting was varied between 10˚C/85%RH and 50˚C/15%RH. A complete cycle was completed in 16 hours. In that time period there was a four hour hold at the lower temperature, followed by four hour ramp to the higher temperature, holding there for four hours, and then followed by a four hour ramp to return to the lower temperature.

A baseline throughput rate was established for each population by averaging the rate over the first 10,000 data packets sent. The duration of this part of the test was approximately one day. The baseline was 93.7 Mbps for the air conditioned environment and slightly less, at 92.4 Mbps, for the temperature cycled environment.

For each population, the authors parsed the data acquired over the remainder of the eight-week period into three

groups representing a 1%, 2%, 5%, 10%, and 20% throughput dropoff compared to the baseline.

Most of the results are plotted in Figure 2. The number of packets at a specified level of dropoff was higher for the population with the free-air-cooled condition. The ratios of these values (averaged over the eight-week period) at the 1%, 2%, and 5% levels, respectively were 2.5:1, 7.3:1, and 14.3:1, respectively. Furthermore, there was a significant increase in the number of packets demonstrating dropoffs of 1 and 2% in the final week of the tests for the temperature cycled population.

There were no packets in the air conditioned environment at the 10% and 20% dropoff levels. However, for the harsher environment there were 105 and 55 packets, on the average, per week.

The authors concluded that the level of performance variation of the switch in the simulated free air cooled environment might well be unacceptable to many data center customers.

CONCLUSIONS

This article highlights a number of published studies that address performance problems related to moisture absorption in individual electronic components and in subsystems. In the experience of this author, the majority of moisture-related studies have to do with reliability not performance. Indications are that the relaxed temperature and relative humidity ranges approved by ASHRAE will some day become the norm in the datacenter. There is a risk that electronics companies will not anticipate the effect this change may have in the high-speed performance of their products. This situation could be exacerbated by the fact that performance degradation might well occur as soon as the moisture concentration achieves a critical value without the need for a secondary process to be triggered by the moisture absorption, as is usually the case with failure mechanisms.

It is hoped that this article will help to increase awareness of these issues in our industry and promote early action to effectively manage the risks detailed here.

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Estimating Internal Air Cooling Temperature Reduction In a Closed Box Utilizing Thermoelectrically Enhanced Heat Rejection

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AN EARLIER article in this column considered the problem of cooling electronic components in a closed box [1]. In outdoor applications for example, it may be necessary to totally seal the box to prevent exposure to airborne particulates, water droplets or other substances in the air that could be injurious to the electronic components. In such an application, heat picked up by the air circulating over the electronic components within the box is rejected to outside air by means of an air-to-air heat exchanger mounted in one of the walls of the box. Such a heat exchanger may be as simple as two plate-fin heat sinks (or a heat sink with fins on both sides) mounted base to base in an opening in the wall of the box. Of course in such cases, the air that is cooling the electronics components will always be higher in temperature than the outside air being used for heat rejection from the box. If this does not provide a satisfactory cooling solution, an alternative that might be considered is augmentation with thermoelectric cooling (TE) modules sandwiched between the heat sinks as shown in Figure 1.

For those that are unfamiliar with TE modules, a thermoelectric cooler, sometimes called a Peltier cooler, is a solid-state heat pump that transfers heat from one side of the device to the other side depending on the direction of the applied electric current [2,3]. For example in Figure 1, electric current, I, may be applied to the thermoelectric modules such that the side in contact

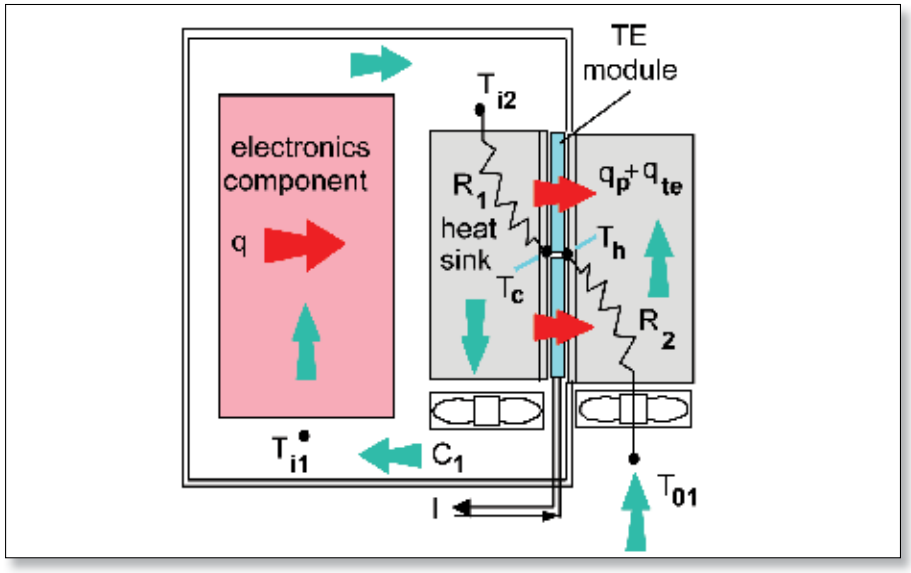

FIGURE 1: Closed box electronics enclosure with thermoelectrically enhanced heat rejection.

with the base of the heat sink within the box becomes cooler, thereby augmenting the transfer of heat from the air circulating within the box to the internal heat sink. The opposite side of the thermoelectric module becomes hotter and both the heat pumped by the thermoelectric cooler (q_p), and the heat dissipated (q_{te}) by the thermoelectric cooler in performing its heat pumping function, is transferred to outside cooling air via the external heat sink.

This article is intended to present to the reader, by example, a methodology to estimate the cooling air temperatures that can be achieved by thermoelectric augmentation. However, to illustrate the value of thermoelectric augmentation, we will first consider some equations to calculate the air temperature (T_{i1}) entering the portion of the box housing the electronic components without thermoelectric augmentation. Working from the air temperature (T_{01}) outside the box to the temperature of the wall (T_w) of the box (or a base temperature common to the external and internal heat sinks) gives,

$$(1)\quad T_w = T_{01} + qR_2$$

where q is the heat dissipation of the electronic components and R_2 is the total thermal resistance of the external heat sink, neglecting the contribution of the rest of the wall. It should be noted that throughout this analysis and in the subsequent calculation examples, heat sink resistances, R_1 and R_2, are assumed to include both the convective part and

any associated thermal interface resistance between the heat sinks and the wall or later in the article, the TE modules. The air temperature entering the internal heat sink passages is given by,

(2) $T_{i2} = T_w + qR_1$

which, substituting in eq. (1) for T_w, gives

(3) $T_{i2} = T_{01} + q(R_1 + R_2)$

The temperature drop of the air passing through the internal heat sink is given by,

(4) $T_{i2} - T_{i1} = \frac{q}{C_1}$

where C_1 is the air heat capacity rate inside the box, given by the product of the mass flow rate, $\dot{m}$, and specific heat, c_p, of the inside air cooling stream. So, the temperature, T_{i1}, of the cooling air entering the electronics compartment (without thermoelectric augmentation) becomes,

(5) $T_{i1} = T_{01} + q(R_1 + R_2) - \frac{q}{C_1}$

Now, we will proceed to determine the temperature of the air entering the electronics compartment when thermoelectric cooling augmentation is incorporated. To do this we must include equations to account for thermoeletric heat pumping and the heat dissipation of thermoelectric modules. In an earlier article, Luo [4] presented the following equation for heat pumping with a thermoelectric cooling module

(6) $q_p = S_m T_c I - \frac{1}{2} I^2 R_m - K_m(T_h - T_c)$

and another equation for the corresponding TE heat dissipation

(7) $q_{te} = IS_m(T_h - T_c) + I^2 R_m$

in terms of the TE parameters at the module as defined in the nomenclature and discussed by Luo [4]. It should be emphasized here that the temperatures, T_h and T_c, in equations (6) and (7), as well as in equations (6a) and (7a) to follow, must be expressed in Kelvin temperature units (i.e. Kelvin temperature = Centigrade temperature + 273.16).

In addition to the above two thermoelectric equations we have the following heat transfer equations,

(8) $q = C_1(T_{i2} - T_{i1})$

(9) $T_c = T_{i2} - qR_1$

(10) $T_h = T_{01} + (q - q_{te})R_2$

It should be noted here that under steady-state conditions heat load, q, in equations (8-10) is equal to the heat pumped, q_p, by the thermoelectric cooler. Considering equations (8–10) together with thermo-electric equations (6) and (7) we have five linear algebraic equations. Given that we know or can assume values for q, R_1, R_2 , C_1, S_m, K_m, R_m and I, we are left with five unknown variables. The unknown variables are q_{te}, T_h, T_c, T_{i2} and T_{i1} (which is the variable we are really after). It is possible to solve these equations via algebraic substitution, as the author has done with the aid of software [5] capable of performing symbolic algebraic manipulation. However, the author found that the algebraic solution obtained for T_{i1} by this method was so long (about two or three screen-widths) and so complex as to be of practically no value other than demonstrating that a solution could be obtained.

A method of practical utility is to solve these equations for numerical values using a matrix method as employed in an earlier article addressing the solution of a thermal resistance network [6]. To do this we first rearrange the equations (6-10) so that the unknown variables are on the left-hand side of the equation and the constant terms are on the right-hand side,

(6a) $S_m T_c I q_p - K_m T_h + K_m T_c = q + \frac{1}{2} I^2 R_m$

(7a) $q_{te} - IS_m T_h + IS_m T_c = I^2 R_m$

(8a) $C_1 T_{i2} - C_1 T_{i1}) = q$

(9a) $T_c - T_{i2} = -qR_1$

(10a) $T_h - q_{te}R_2 = T_{01} + qR_2$

In matrix notation these same equations can be compactly represented as

(11) **[Coeffs] x [Unknowns] = [Constants]**

TABLE 1: NOMENCLATURE

q_p	=	Heat pumped by TE modules
q_{te}	=	Heat dissipation of TE modules
q	=	Electronics heat dissipation in box
T_h	=	TE module hot side temperature
T_c	=	TE module cold side temperature
T_{01}	=	Air temperature outside box
T_{i1}	=	Air temperature into electronics package
T_{i2}	=	Air temperature out of electronics package
T_w	=	Base temperature of heat sink(s) w/o TEs
I	=	Electric current supplied to TE module
S_m	=	TE module effective Seebeck coefficient
K_m	=	TE module thermal conductance
R_m	=	TE module electrical resistance
R_1	=	Thermal resistance of cold side heat sink
R_2	=	Thermal resistance of hot side heat sink
C_1	=	Air heat capacity rate within box ($\dot{m}c_p$)

The coefficients of the unknown variables and the corresponding constant terms for each equation may be grouped in a tabular form as shown in Table 2. So doing, the top row represents the column vector of unknowns, the columns beneath each unknown variable make up the coefficient matrix and the rightmost column the constant vector.

The coefficient matrix below comprises the known coefficients of the unknown variables of the equations, as shown in Table 2,

$$\text{Coeffs} = \begin{bmatrix} 0 & 0 & S_m + K_m & 0 & -K_m \\ 0 & 0 & I\,S_m & 1 & -I\,S_m \\ -C_1 & C_1 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & -R_2 & 1 \end{bmatrix}$$

the column vector of unknown variables which we seek to solve is,

$$\text{Unknowns} = \begin{bmatrix} T_{i1} \\ T_{i2} \\ T_c \\ q_{te} \\ T_h \end{bmatrix}$$

and the column vector comprising the known constants on the right hand side of each equation is,

$$\text{Constants} = \begin{bmatrix} q + I^2R_{m/2} \\ I^2R_m \\ q \\ -qR_1 \\ T_{01} + qR_2 \end{bmatrix}$$

A matrix equation such as (11) may be solved for the unknown variables by multiplying the constant vector by the inverse of the coefficient matrix,

(12) **[Unknowns] = [Coeffs]$^{-1}$ x [Constants]**

Many computational aids such as MathCad [5], Matlab [7], and EXCEL [8] can be used to obtain the matrix inverse of the coefficient matrix and multiply by the constant vector to obtain the desired solution vector.

To demonstrate the potential enhancement with thermoelectrically augmented cooling, we now turn our attention to some numerical results obtained using the method described above. For purposes of illustration, a small enclosure with an allowable opening in one side of 100 mm x 100 mm is assumed. It is further assumed that the base dimensions of the internal and external air-cooling heat sinks are 100 mm x 100 mm. Before proceeding further it is necessary to assign values to the thermoelectric module cooling parameters, S_m, K_m,and R_m. The same 40 mm x 40 mm TE module considered by the author in an earlier article [9] will be considered here. In the earlier article, the author illustrated the calculation of single module TE parameters from vendor data, using the method discussed by Luo [4]. The values for the example TE module were found to be:

$$S_m = 0.068 \text{ V/K}$$
$$K_m = 0.712 \text{ W/K}$$
$$R_m = 2.307\ \Omega$$

However, to increase the overall heat pumping capacity, four of these TE modules can be sandwiched in a 2 x 2 array between the bases of the internal and external heat sink. Consequently, the parameters for the array of TE modules will simply be four times the value for a single TE module or,

$$S_m = 0.272 \text{ V/K}$$
$$K_m = 2.848 \text{ W/K}$$
$$R_m = 9.228\ \Omega$$

Also, if we assume that the TE modules are wired in series, the current, I, through each module will be the same and equal to the total current.

Calculations were performed for a range of heat sink resistances to show the effects of this parameter, coupled with the thermoelectric cooling effects. The heat sink thermal resistances used in the calculations were 0.075, 0.125 and 0.175 oC/W and were considered to have the same value for the heat sink within and outside the box (i.e. $R_1 = R_2$). The internal air flow rate within the box was assumed to be 20 CFM (0.00944 m^3/s).

As noted earlier equations (6) and (7) are in Kelvin temperature units. Therefore, the temperature of the outside cooling air, T_{01}, used in the calculations, must also be in degrees Kelvin and the temperatures obtained from equation (12) will be in degrees Kelvin. However, for ease of understanding, the temperatures reported in the following figures have been converted to degrees Centigrade.

Figure 2 illustrates both the effect of increasing electric

TABLE 2: COEFFICIENTS OF UNKNOWN VARIABLES AND CONSTANTS IN EQUATIONS

T_{i1}	T_{i2}	T_c	q_{te}	T_h	Constant
0	0	$S_m + K_m$	0	$-K_m$	$q + I^2R_{m/2}$
0	0	$I\,S_m$	1	$-I\,S_m$	I^2R_m
$-C_1$	C_1	0	0	0	q
0	-1	1	0	0	$-qR_1$
0	0	0	$-R_2$	1	$T_{01} + qR_2$

current through the TE modules and heat sink thermal resistance, with a heat load of 100 watts from the electronics and an outside air temperature of 35 °C. The solid lines represent the cooling air temperature, T_{i1}, within the box with the TE modules sandwiched between the heat sinks and the dashed lines represent the temperatures obtained without the TE modules. As can be seen, at low values of electric current, the presence of the TE modules result in higher cooling air temperatures within the box. This is because at low electric current, the Peltier heat pumping effect is offset by the thermal resistance across the TE modules. As current is increased the Peltier heat pumping effect becomes more significant and the inside cooling air temperature can be decreased significantly. However, as electric current continues to be increased, the Joule heating (i.e. heat dissipation) within the TE modules becomes increasingly significant causing the inside cooling air temperature to bottom out and then begin to rise if current is increased still further.

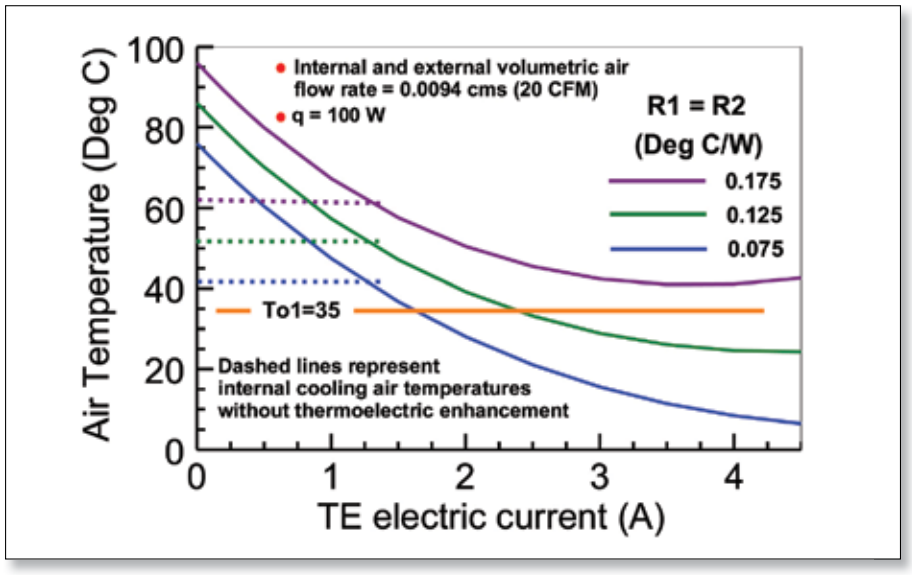

FIGURE 2: Effect of increasing electric current to TE modules on internal cooling air temperature.

Figure 3 illustrates the effect of the electronics heat dissipation on cooling air temperature within the box, with a constant current of 3.5 amperes through the array of TE modules and an outdoor temperature of 35 °C. The internal and external air flow rate was held constant at 0.0094 cms (20 CFM). As can be seen, for the heat load range considered for this analysis, the cooling air temperatures obtained in all the cases are lower than could be achieved without employing TE enhancement. It should also be noted that, depending on heat load and heat sink thermal resistance, in many cases the cooling air temperature is even lower than could be obtained using outside air for cooling.

The results in Figure 4, show the effect on cooling air temperature within the box, of supplying a fixed current of 3.5 amperes to the TE modules and for a fixed electronics heat load of 100 watts. It can be seen that in this case, the resulting cooling air temperatures are always below the cooling air temperatures that could be achieved without thermoelectric enhancement.

The equations and solution methodology presented in this article can provide a useful tool with which to obtain a preliminary estimate of the effectiveness of thermoelectric augmentation in providing cooling to electronic components in a closed box.

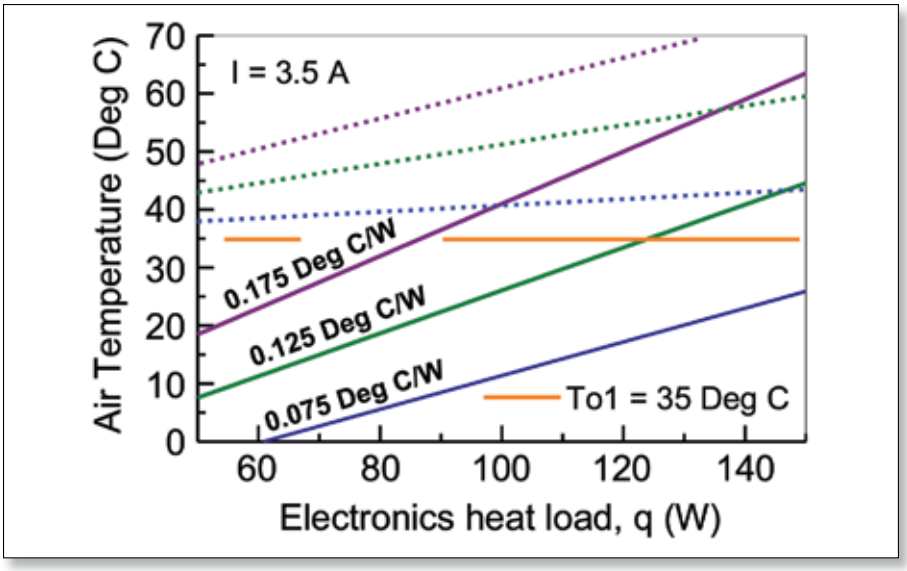

FIGURE 3: Effect of electronic heat load on internal cooling air temperature with (solid lines) and without (dashed lines) thermoelectric augmentation.

Of course when considering the use of thermoelectrics for cooling applications, the designer should be cognizant of the electrical power required to drive the thermoelectric elements, which is given by equation (7). The cooling efficiency of thermoelectric devices relative to their power consumption, as with other types of heat pumping devices, may be characterized in terms of Coefficient of Performance (COP). COP is defined as the ratio of cooling (q) provided over the electrical energy consumed (q_{te}) to produce the cooling effect. For example, for the results shown in Figure 3, the COPs ranged from 0.3 to 0.4 at heat loads of 50 or 60 W to around 1 at a heat load of 150 W. The range of heat sink thermal resistance values had only a little effect on the COP realized. Similarly, considering the results shown

in Figure 4, COPs ranged from 0.6 to 0.7 with little effect due to heat sink thermal resistance or outside air temperature. As one might expect from equation (7) the principal effect on COP is caused by the electrical current required to drive the thermoelectrics. This is amply demonstrated considering the results presented in Figure 2. At electric currents around 1.25 A, the COPs calculated ranged from 6 to 6.4 depending on the value of heat sink thermal resistance. Although these COPs may seem good, in this case the cooling air temperature within the box is no lower than could be achieved without thermoelectrics. As current is increased in Figure 2, the COP realized decreases rapidly to about 0.65 at a current of 3.5 A. However, even though the COP has dropped, this coincides with the maximum reduction of air temperature within the box by as much as 20 to 30 Centigrade degrees below those achieved without thermoelectric augmentation. For comparison, the COP values realized by conventional vapor compression refrigeration systems may typically vary from 1 to 4.

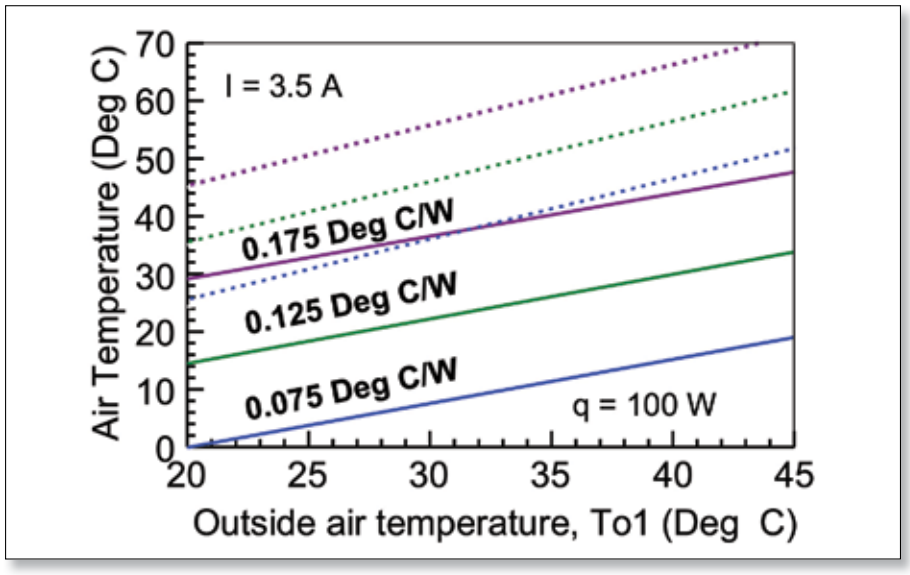

FIGURE 4: Effect of outside air temperature on internal cooling air temperature, Ti1, with (solid lines) and without (dashed lines) thermoelectric augmentation.

Finally, it should be noted that a number of vendors provide thermoelectric heat exchangers for cooling air within in a closed box. The interested reader may find a number of vendor products and examples by conducting an internet web search using the terms "thermoelectric air cooler" or "thermoelectric air conditioner."

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Thermal Spreading
and More Using Open-Source FEA Software

Gordon Ellison
Tektronix, Inc., Retired

THE PURPOSE of the present article is to suggest that accurate solution of thermal spreading problems for multilayer, edge-truncated geometry is easily accomplished using free, open-source finite element software. This should be especially attractive to designers and analysts who are full-time independent consultants, temporary contractors, or regularly employed engineers desiring to free themselves from the problems of justifying the cost of infrequently used software. This writer has studied some of the available open-source software and believes that many readers will profit by the information in the following paragraphs.

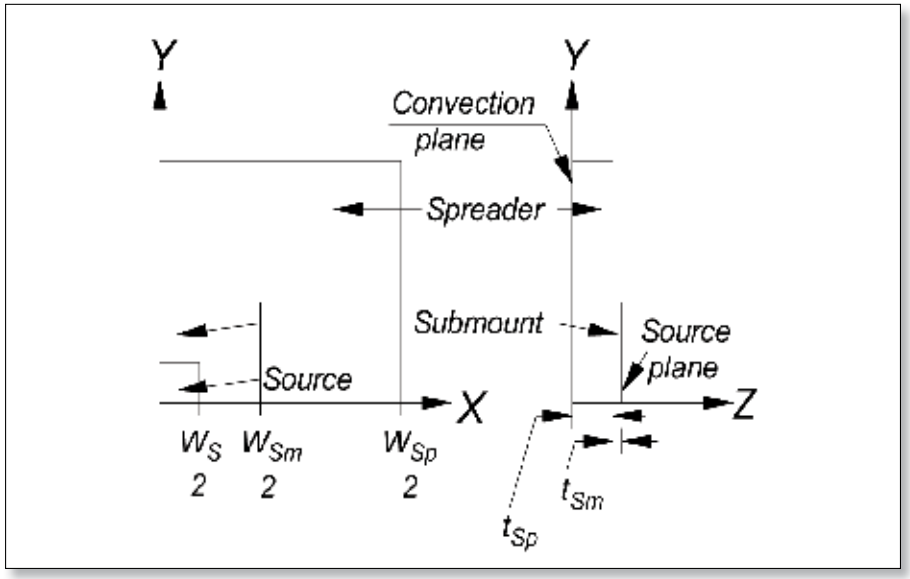

FIGURE 1: Spreader, submount, and source geometry. Planar source is embedded at top surface of submount. One quadrant of square device analyzed.

BACKGROUND.

Thermal spreading resistance is usually defined as the temperature difference per unit heat transfer, e.g. K/W, between a source and a defined isothermal plane, point, or ambient temperature. Math models for steady-state thermal spreading resistance have been under development for several decades. Early models considered conduction to an isothermal reference plane and were therefore of limited use for analyzing electronic packages [1]. Lee described a transistor-on-heat sink application with a convecting and/or radiating surface [2,3]. In this case, a uniform total heat transfer coefficient h was assumed for an ambient temperature T_A. The simplest of these models presumes a circular source centered on the surface of a circular substrate, a model that is accurate for many applications. Ellison published design curves and formulae for the maximum resistance (source center to ambient) for rectangular sources centered on rectangular substrates, either or both with non-unity aspect ratios [4]. Design curves were later added for source-averaged thermal resistances [5]. Time-dependence was added to the rectangular device problem by Rhee and Bhatt [6] who implemented a three-dimensional Green's function solution based on a catalog of solutions by Cole et al. [7].

Gordon Ellison is a retired Tektronix, Inc. Fellow. Following his retirement from Tektronix, he has taught Electronics Cooling at Portland State University and consulted with local companies. His publications include the books *Thermal Computations for Electronic Equipment*, Van Nostrand Reinhold Publishing Co., 1984, reprint edition by Krieger Publishing Co., 1989, and more recently, *Thermal Computations for Electronics,* CRC Press, 2011. He is a past winner of the IEEE Semi-Therm Significant Contributor Award. He received a B.A. degree in physics from the University of California at Los Angeles, and an M.A. in physics from the University of Southern California.

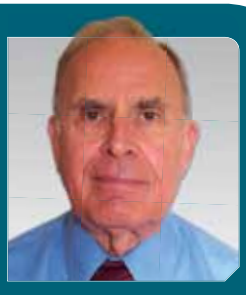

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TABLE 1: VARIABLE PARAMETER VALUES FOR SAMPLE SPREADING PROBLEMS.*						
DEVICE	**PARAMETER**	**CASE 1 (BENCHMARK)**	**CASE 2**	**CASE 3**	**CASE 4**	**CASE 5**
Submount	W_{Sm} / 2 (m)	0.015	0.015	0.0025	0.0015	0.0008
Submount	k_{Sm} (W/m • K)	200	100	100	100	100

*Parameters common to all cases are: spreader K_{Sp} = 200 W/m • K, W_{Sp} / 2 = 0.015 m, t_{Sp} = 2 x 10^{-3} m; submount t_{Sm} = 1 x 10^{-4} m; source W_S / 2= 4 x 10^{-4} m.

Both the steady-state and time-dependent models for three-dimensional conduction problems result in infinite series solutions: a single series for the Lee and Rhee solutions and a double series for the Ellison solutions. While the series formulae are not particularly difficult to implement in a math-scratchpad computer program, there is always the desire to use approximate closed-form formulae, i.e. non-infinite series based. Lee was successful in creating these approximations for his circular-shaped devices [2]. Continuing in the effort to obtain useful modeling results with approximate formulae, Lasance has proposed a method for calculating the spreading resistance for two-layer problems where the layers have unequal dimensions [8,9,10]. In these situations where the planar dimensions of the layers are not equal, there are no established closed-form analytical methods. Consequently, the engineer must often rely on more advanced numerical modeling using finite difference (*FDM*) or finite element (*FEM*) methods. Yovanovich and co-workers have also published numerous studies on spreading and closely related topics [11].

SAMPLE SPREADING PROBLEM GEOMETRY.

Lasance considered the test case of a two-layer spreading problem with a truncated-silicon top layer submount (planar dimensions less than bottom layer), on a copper-tungsten heat spreader as shown in Figure 1 [9]. The source plane is at the top of the submount and all surfaces are adiabatic except the source region and the Z=0 plane, the latter location modeled by a uniform heat transfer coefficient h. Lasance refers to this h as *effective* as it may include the effect of an area-enlarging factor due to a heat sink, a common practice in modeling electronic equipment [5]. In the present problem, h = 250 W/(m²·K), the same value Lasance used for some of his work. An ambient T_A = 0 and a one watt total source dissipation mean that the maximum computed temperature is numerically identical to the thermal resistance. The square source is centered on a square, two-layer substrate, but symmetry allows the analysis of only one quadrant, thus indicating a corner source. Further advantage of symmetry could be used with the *FEA* model by halving this quadrant with a diagonal between the source and opposite corners. Table 1 lists the variable parameters used. A source of 1.0 W is uniformly distributed over the entire source area (8.0x10^{-4} m)² as a heat flux of 1.5625x10^6 W/m².

Case 1 is a benchmark comparison of analytical and *FEA* solutions and is used to justify the *FEA* model mesh for Cases 2-5. The top layer is not truncated for Case 1 and has the same conductivity as the bottom layer, i.e. this is a single layer material. Cases 2-5 are those in which we are primarily interested.

SIMPLE SPREADING CALCULATION FOR CASE 1.

The benchmark calculation for Case 1 uses rectangular device spreading theory from Ellison to obtain the dimensionless source center and source-averaged spreading resistances ψ_{Sp} = 0.59 and $\psi_{Ave\text{-}Sp}$ = 0.50, respectively [5]. Theory shows that the maximum total thermal resistance from the source center to ambient is the sum of terms for one-dimensional conduction, uniform h convection, and spreading [5]:

$$R = \frac{t_{Sp} + t_{Sm}}{k_{Sp} W_{Sp}^2} + \frac{1}{h W_{Sp}^2} + \frac{\psi_{Sp}}{k_{Sp} W_S} = \frac{2x10^{-3} + 0.1x10^{-3}}{(200)(0.03)^2} + \frac{1}{(250)(0.03)^2} + \frac{0.59}{(200)(8.0x10^{-4})}$$

R = 1.167$x10^{-2}$ + 4.444 + 3.688 = 8.14K/W

Similarly, using $\psi_{\text{Ave-Sp}}$, the total source-averaged resistance is R_{Ave} = 7.58 K/W

The source center resistance, R, will be compared with an *FEA* calculation in the Results section.

SOFTWARE USED AND THE SPREADING MODEL DESCRIBED.

Two free of cost, open-source programs were used: (1) Salome [12] and (2) Elmer [13]. In the Windows version, Salome is used primarily for model building and meshing [12]. The Salome software has a rather complete set of plate and solid model features, but is not a complete *CAD* system. Some users might find themselves frustrated by the geometry module, but it is quite adequate for many applications. Perhaps the most inconvenient aspect is that once added, an object's dimensions cannot be changed. Thus if you have an incorrectly sized object, you must delete it and try again. This is not much of a problem and if you prefer, an open-source *CAD* program is also available [14].

In the current spreading problem, Salome was used to

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build, mesh, and export the models. A look at Figure 2 for Case 3 shows that each model is constructed from three-dimensional blocks: a submount block, a spreader block, and a source block, the latter superimposed at a corner. The submount planar dimensions all differ for Cases 2-5. However, Cases 3-5 have truncated submount dimensions, i.e. the submount does not fully extend out to the spreader edges – a problem that is not managed by any of the analytical solutions of Ellison and Lee.

The source block has a total thickness that is the sum of the submount and spreader thicknesses. The top surface of the source block is the region to which the heat flux is applied (colored red in Figure 2). If the source, submount, and spreader blocks were left as-is in Salome, the geometry would consist of a single material. The "Geometry-Partition" operation must be used to separate the system into the three distinct objects. A later operation, "Geometry-Group" or "Mesh-Group," is used to combine the lower portion of the source block with the spreader, and also to combine the upper portion of the source block with the submount, resulting in two distinct material groups. Two extruded circles are used to permit the creation of submesh regions with finer detail than that for the overall system. One of these cylinders is visible in Figure 3. Note that the mesh in Figure 2 shows the finest mesh in the source region, a not quite so fine mesh throughout the submount dimensions, and an even coarser mesh for the remainder of the spreader.

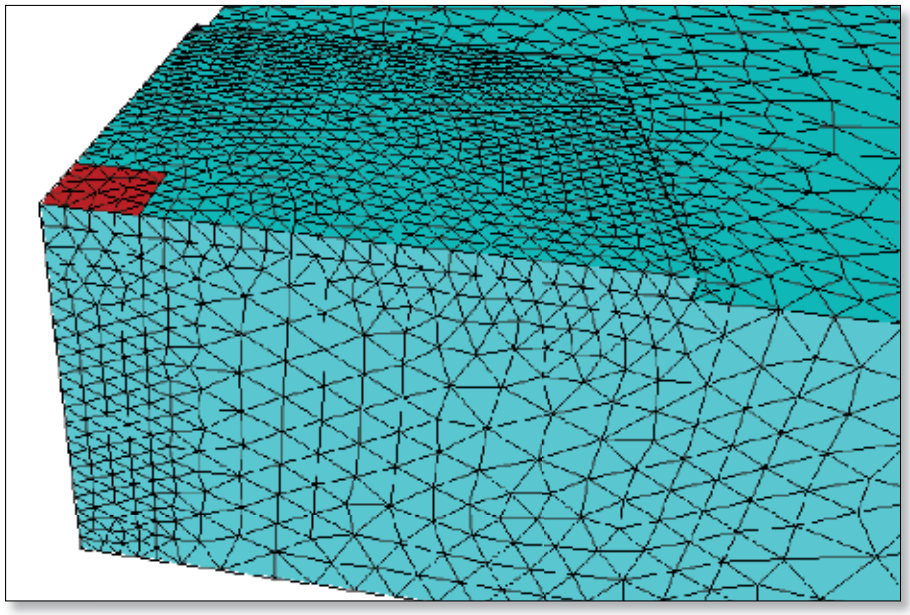

FIGURE 2: Case 3 mesh for source, truncated submount, and a portion of the spreader. Source plane shown in red.

An "Explode" option is used to identify the various solid blocks and faces that can be grouped into the two different materials as well as the source and convection faces. The geometry and meshing efforts are completed by exporting the mesh to some suitable file structure, a good choice being the universal UNV type. The next step is to convert this file to a mesh file that is recognizable by the solving program, Elmer [13]. The file converter is a command-type program known as "Elmergrid." This program not only creates the correct input file for Elmer, but can also be used to clean up the UNV file.

The mesh file is loaded into Elmer, which has a very complete set of options for input, in this case heat conductivities, heat flux, and the heat transfer coefficient. The project is saved to the hard drive and a simple click of a solver icon begins the solution process. Once a successful solution is obtained, one can use either of two different Elmer options to display results. For example, the "run-vtk" post-processor was used to produce Figure 3.

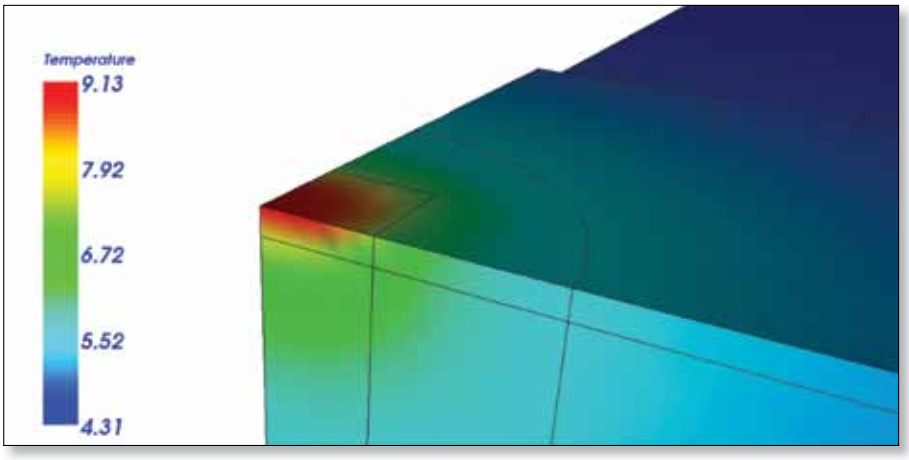

FIGURE 3: Case 3 *FEA* results.

SPREADING RESULTS.

The theoretical and *FEA* results are listed in Table 2. The Case 1 benchmark, Theoretical and *FEA* results, have a discrepancy of 0.5%. The Case 1 theoretical and *FEA* discrepancy for the third term, $R_{Sp} = \psi_{Sp}/kW_S$, of the total resistance is 1.2%. These discrepancies are sufficiently small to justify the mesh. Note that for Cases 2-5 the resistance increases only slightly as the heat spreader planar dimensions decrease. A portion of the Case 3 thermal surface contours in the vicinity of the source is shown in Figure 3, for which the legend is left with non-integral values so that the maximum temperature, i.e. the resistance, is dis-

TABLE 2: THERMAL RESISTANCE FOR SAMPLE SPREADING PROBLEM

PARAMETER	CASE 1 THEORETICAL* (BENCHMARK)	CASE 1 *FEA* (BENCHMARK)	CASE 2 *FEA*	CASE 3 *FEA*	CASE 4 *FEA*	CASE 5 *FEA*
k_{Sm} (W/m • K)	200	200	100	100	100	100
W_{Sm} / 2 (m)	0.015	0.015	0.015	0.0025	0.0015	0.0008
R(K/W)	8.14	8.10	9.09	9.13	9.15	9.18

*Refers to the section entitled "Simple Spreading Calculation for Case 1."

played. In this case the submount is about six times the size of the source dimension and it is very clear that the size of the submount can be substantially decreased without significantly increasing the thermal resistance. The smallest submount configuration evaluated has dimensions of only twice those of the source and yet the thermal resistance is hardly different than that for Case 2, which has a non-truncated submount. These observations are entirely consistent with the surface temperature colors in Figure 3. The analysis also demonstrates the advantage that graphical results have over the single-value "theoretical" calculation used for the benchmark.

With regard to studies by Lasance in an evaluation of the application of single layer spreading formulae to multilayer problems, we can see in Figure 3 that use of the submount dimensions considered herein as a source for the second layer would be a poor modeling choice because such source dimensions would be too large.

No attempt has been made to address model approximations, but one of the omissions in this study is the absence of convection cooling from the submount and spreader planes on the source side of the device. This feature would be easy to add to the *FEA* model.

MORE COMPLEX CONDUCTION PROBLEM – SINGLE CHIP PACKAGE ON *PCB* COUPON.

The thermal spreading problem considered in the preceding paragraphs has very simple geometry. As an example of a more complex problem, a single chip package attached to a circuit board coupon is shown with results in Figure 4. The geometry was constructed using the "Free-cad" open-source software [14]. While the author of this software stipulates that the program is under continuous development, it was more than sufficient for this problem and makes up for the limited model construction capabilities of Salome. In particular, it is helpful that Free-cad object dimensions are easily modified. The Free-cad STEP file export feature was used to create a file for import into Salome. From that point on, geometry meshing and model solving is similar to procedures used in the spreading example. Note that the substrate geometry was submeshed to obtain a finer mesh. The heat dissipating chip is not visible because it is mounted on the underside of the substrate.

The legend for the *IC* package results in Figure 4 is left with non-integral values so that the maximum temperature (at chip source center) is displayed. This same problem was constructed and analyzed with commercial *CAD* and *FEA* software, for which the model and results are shown in Chapter 1 of [5]. The two different *FEA* programs were used to obtain a maximum temperature rise above ambient with about one percent discrepancy, a value that is probably due to mesh differences.

SUMMARY AND COMMENTS.

The *FEA* method permits the analysis of geometry that is too complex for analytical spreading formulae, most of which are infinite series solutions that cannot accurately account for multilayer structures with one or more edge-truncated layers. The chip package on *PCB* in Figure 4 is a moderately complex example solvable using most *FEA* codes. The reader inexperienced in *FEA* is cautioned to check for grid independence of the numerical solution, particularly when there are large scale differences in the geometry.

Details of using the open-source software have been largely omitted in this article because of space limitations. However, it is hoped that the reader will be pleased to learn of the programs introduced. The web can be searched for tutorials, though some of these may not be in the field of interest. Nevertheless, there may be sections of any tutorial that are of general use for modeling and meshing. In particular, there are many Elmer tutorials provided as part of the download package. The number of Salome tutorials is more limited. Finally, don't let the name "Free-cad" lead you to think that it is not a serious program. Though it may not yet meet the needs of someone requiring a commercial grade tool, it is still very useful. The Appendices will be of interest if you choose to evaluate the software for yourself.

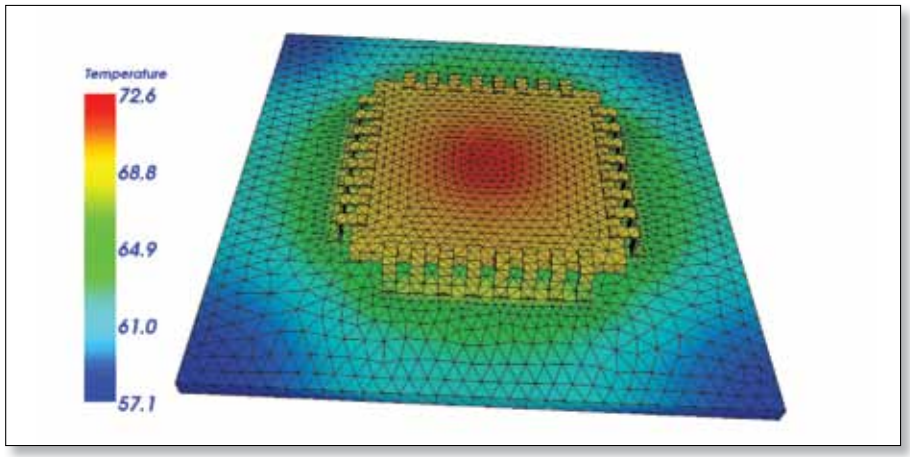

FIGURE 4: Temperature rise above ambient for a single chip package on *PCB*. IC chip hidden at base of inverted substrate. Circuit board dimensions: 50.08 mm *x* 50.08 mm *x* 1.52 mm with orthotropic *k*. Ceramic substrate dimensions: 25.4 mm *x* 25.4 mm *x* 1.27 mm. Chip dimensions: 5.08 mm *x* 5.08 mm *x* 0.51 mm. All surfaces use h = 15.5 W/m^2 ·K. Chip dissipation is 3.0 W or 116,250 W/m^2.

APPENDIX I: SALOME OPTIONS AND SUGGESTIONS.

1. In the Salome menu bar, you will need to select Geometry or Mesh from the drop down Salome list, depending on what you want to do.
2. When you create your first geometric entity or load a *CAD* file, you need to right click on Geometry and select "Show" in the Object Browser to visualize the problem. You will also have to click on a "magnifying glass" icon to fill the display window. A similar procedure applies to viewing a mesh.
3. Geometry - Operations - Partition: you need this operation to separate the various geometric blocks into distinct parts, which otherwise will be a single material.
4. Geometry - New Entity - Explode: use this to "explode" the various geometric entities into solid parts and faces, the latter being necessary to apply boundary conditions.
5. Mesh - Create Mesh - Algorithm (use Netgen 1D-2D-3D): in the Object Browser, select your partition (Partition_1 by default) on which to create the mesh.
6. Compute: in the Object Browser, right click Mesh_1 (the first default name) and select "Compute."
7. While in the Mesh option, create mesh groups to isolate individual materials and boundary faces.
8. Note that in Figure 4 the substrate has a different mesh density than the *PCB*. This was constructed by first creating the overall mesh, selecting Mesh_1, then selecting Mesh-Create Submesh option (with a greater mesh density), and right clicking Mesh_1 and selecting Compute. The submesh parameters can be edited and the problem remeshed without beginning again.
9. Export to UNV file: do this by right clicking Mesh_1 in the Object Browser and making the selection.

APPENDIX II: ELMER OPTIONS AND SUGGESTIONS.

1. After you install Elmer, you may need to drag an ElmerGUI.exe to create a desktop shortcut icon.
2. Add a path to the Elmer executable, Elmergrid: Using Windows Explorer, select Computer, Properties, Advanced System Settings, Advanced, Environment Variables, Path, Edit, and then add the path to the Elmer installation directory. This will let you run "elmergrid" from any Command Prompt in any directory.
3. Create a desktop Command Prompt for convenience.
4. Use the Command Prompt to change to your model file drive and directory, then run Elmergrid without any arguments to get a list of options. A suggestion is to use "elmergrid 8 2 mesh_1.unv -autoclean," where mesh_1.unv is the model mesh file.
5. In your first use of a mesh file, use Elmer - File - Load Mesh: select the folder "mesh_1" that was automatically created when you used Elmergrid. Don't be confused by looking for a file. Elmer requires that you select a folder, not a file.
6. When you input model details for a heat problem, don't forget to select Model - Equation - Add Heat Equation, and check the Active option.
7. After you have successfully solved a problem, if you use the Elmer "Post" icon, you may need to edit the background color to see all of the legend numbers.

APPENDIX III: OTHER SUGGESTIONS.

1. Free-cad, Salome, and Elmer are available as Windows binaries. Issues with regard to Windows 8 are presently unknown to the author.

2. The Ubuntu Linux distribution is easily downloaded as an ISO file, which in turn can be used to create a Linux boot-able system on a USB flash drive or DVD [15]. This distribution contains a large number of applications in addition to Free-cad, Salome, and Elmer. There is a Salome-Meca program that includes heat and elasticity modules, but the lack of complete manuals and the use of the French language in some parts of the software present obstacles for non-French readers.

3. The Linux CAE distribution is an alternate to MS Windows.

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This list of references is not all-inclusive as there are other publications to be found on the subject.

Two-Phase Flow Control of On-Chip Two-Phase Cooling Systems Developed for Blade Servers of Data Centers

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NOMENCLATURE
COP = coefficient of performance
CPU = central processing unit
LP cycle = liquid pumped cycle
ME = microevaporator
MIMO = multiple input multiple output
VC cycle = vapor compression cycle
PI = proportional integral
SIMO = single input multiple output
SISO = single input single output
SMV = stepper motor valve

SERVER MANUFACTURERS and data center managers are showing a greater concern regarding the energy efficiency and cooling of the new generation of servers for data centers. With very large data centers exceeding 100,000 servers, some even consuming more than 50 MW [1] to operate, this electrical energy is directly converted to heat and then simply "wasted" as it is dissipated into the atmosphere.

A recent solution to this "energy crisis" adopted by thermal designers of data centers is the confinement of the air cooled servers inside of racks with air-to-water cooling coils for heat removal, as an attempt to maximize the cooling performance and to reduce the overall thermal resistance between the chip and the external environment. Another solution is relying on the use of outside cold air and/or water for cooling (i.e., free cooling [2]), which is highly dependent of external environment conditions, and requires additional components, such as filters, ducts and fans, dampers, etc. This solution requires high levels of specialized controllers, continuous maintainance and is susceptible to errors [3].

A long-term solution is to upgrade to on-chip two-phase cooling [4], which besides providing very high cooling performance at the chip level without requiring a heat spreader with a large footprint, also eliminates the poorly performing air as a coolant altogether [5, 6] and adds the capability to reuse the waste heat in a convenient manner, since higher evaporating and condensing temperatures of the two-phase cooling system (evaporating its dielectric refrigerant at the chip at temperatures up to 60°C whilst still maintaining the chip comfortably below 85°C) are possible with such a new green cooling technology.

Single-phase (water) on-chip cooling technologies have been implemented in new supercomputers, showing reductions in power consumption up to 45% when compared with air cooling technologies [7]. On-chip cooling has also yielded a significant increase in computing performance in terms of computing throughput (lower chip

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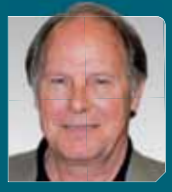
Prof. John Richard Thome has been working at the Swiss Federal Institute of Technology Lausanne (EPFL) since 1998, where he is a director of the Laboratory of Heat and Mass Transfer (LTCM) and the director of Doctoral Program in Energy (EDEY). He received his Ph.D. in mechanical engineering at Oxford University in 1978 and worked as an assistant/associate professor in the US for five years at Michigan State University. He worked full-time as a consulting engineer for 15 years from 1984 through 1998 with his own firm. He has more than 170 journal papers and four books since joining the EPFL. His current main areas of research are two-phase flow and heat transfer in microchannels, two-phase flow control for electronics cooling using new hybrid cooling cycles; using either speed control of oil-free pumps and compressors or passive systems such as thermosyphons, and energy recovery systems.



temperature, lower gate current leakage, lower voltage and higher frequency) and computing throughput per electrical energy use. Thus, the appeal here is to improve even more the computing performance using two-phase on-chip cooling, which due to the latent heat of the coolant, removes much higher heat fluxes while requiring smaller coolant flow rates than in the single-phase cooling [8]. Better temperature uniformity across the chips is also achievable.

In the present work (condensed version of the paper presented in [4]), two such two-phase cooling cycles using micro-evaporation technology were experimentally evaluated with specific attention being paid to energy consumption, overall energetic efficiency and more specifically controllability. The cooling cycles were comprised of a tube-in-tube counter flow condenser (heat rejection), two parallel micro-evaporator (ME)/pseudo chip packages (mimicking the cooling of the chips of blade servers) and a stepper motor valve (SMV) at the inlet of the MEs for flow control reasons. The two alternative drivers tested were a mini-vapor compressor (VC cycle) and a gear pump (LP cycle). Additionally, two internal heat exchangers were considered in the VC cycle to guarantee subcooling at the inlet of the MEs and superheating at the inlet of the minicompressor.

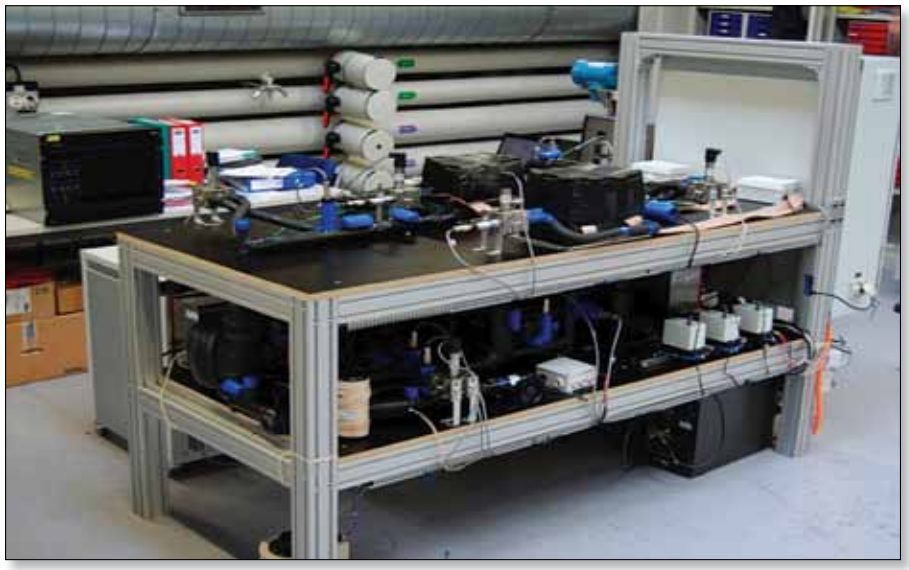


FIGURE 1: Hybrid cooling system test bench.

Figure 1 shows the multi-purpose test bench constructed to experimentally evaluate the performance of these cooling systems under various typical blade server operating conditions of transient, steady-state, balanced and unbalanced heat loads on the system's two pseudo CPU's. More details about the different cooling loops can be found in [9]. Since limited experience is available on two-phase cooling flow control for servers, this was the major objective to demostrate here, implementing simple controllers.

FLOW CONTROL

The operational goal here is to maintain the chip temperature below a pre-established level by controlling the inlet conditions of the micro-evaporator cold plate (pressure, inlet subcooling and mass flow rate). Futhermore, it is imperative to keep the ME's outlet vapor quality below that of the critical vapor quality, which is associated with the critical heat flux (premature dry out in the channels). Notably, the coolant flow rate is modulated to control the exit vapor quality to a target value and thus match the heat load fluctuation during the chips' operation. Hence, greatly reduced energy consumption of the driver during normal operation and providing low energy consumption during standby operation and also *off* capability when the server is not in operation for even greater energy savings.

The condensing pressure must also be controlled since it sets the saturation temperature of the coolant. If the aim is to recover the energy dissipated by the coolant in the condenser to heat buildings, residences, district heating, pre-heat boiler feedwater, etc. (here represented by a thermal bus), this can be achieved using either a compressor (VC cycle) to reject the waste heat at a higher temperature (at the cost of higher energy consumption) or using a pump (LP cycle) to reject the heat at the ME's exit saturation temperature, both

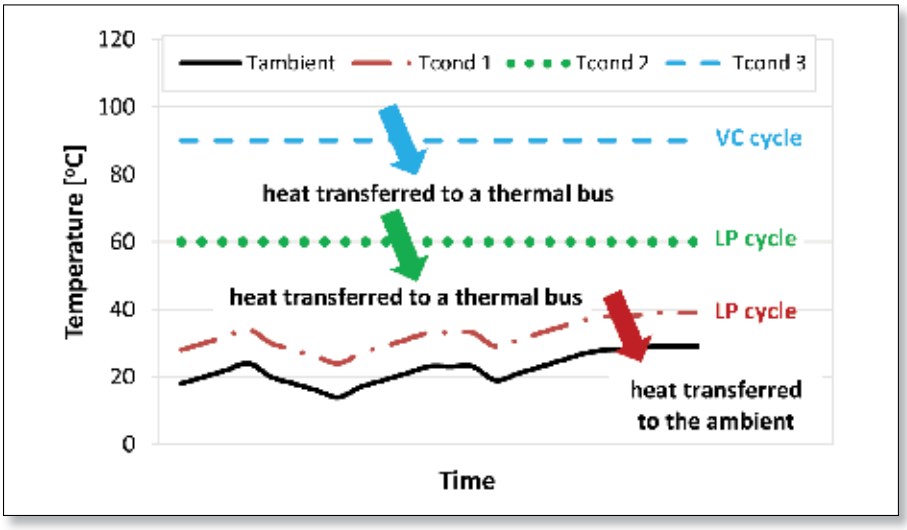


FIGURE 2: Condensing temperature control considering (or not) waste heat recovery.

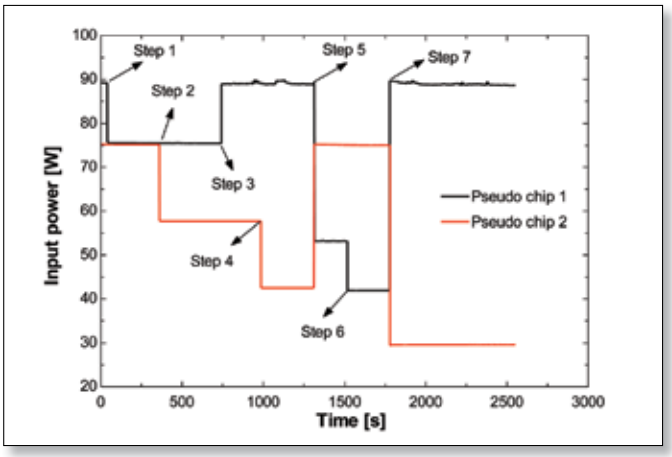


FIGURE 3: Different heat loads on the MEs.

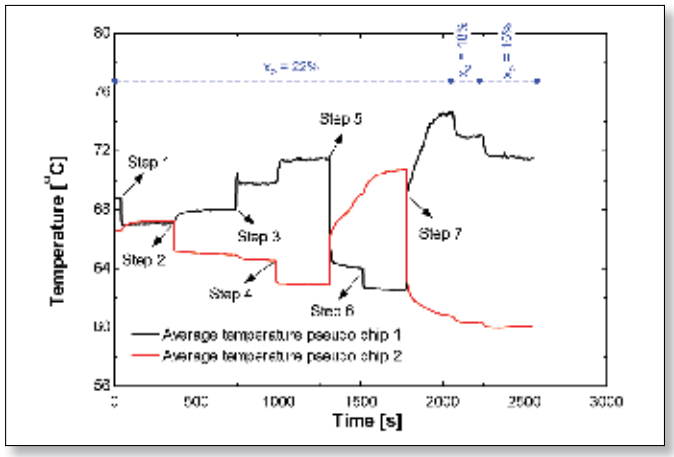


FIGURE 4: Average temperatures on the pseudo chips.

without requiring any refrigeration chiller. Otherwise, using a pump as the driver, the ME's exit saturation temperature can be modulated to follow the outside air temperature for heat dissipation into the ambient air via a compact air-cooled heat exchanger (*viz.* Figure 2).

For the experimental evaluation, specific controllers were first designed and tested [9]. The variables controlled here were the ME's outlet vapor quality, the condensing pressure (LP cycle) and the approach temperature in the condenser (VC cycle). The actuators used were a variable stroke length oil-free vapor compressor, a variable speed condenser water pump and an electronically controlled stepper motor valve (over-dimensioned to modulate the refrigerant mass flow with a negligible pressure drop).

Two ME's in parallel (typical for blade server boards) assembled on two pseudo chips to emulate actual ones, each composed of 35 heaters and temperature sensors (2.5 mm by 2.5 mm in size made from a Delphi thermal test die), were used. The ME's copper microchannel geometry consisted of 53 parallel channels having a height of 1.7 mm and a width of 0.17 mm, with the fins between channels being 0.17 mm thick. The effective "footprint" area of the ME's is 12 mm length from inlet to outlet and 18 mm width. In the present work only uniform heat fluxes were considered and HFC134a (a common refrigerant that is a dielectric fluid) was tested as the working fluid

Finally, for the present experimental campaign, only one SMV was considered for modulating the flow to both MEs. The outlet vapor quality used for control was that at the exit after both flows from the ME's are mixed. The condenser used water as the secondary fluid, where the driver was a controllable speed gear pump.

EXPERIMENTAL RESULTS

Experiments for set point tracking (for each controller developed), disturbance rejection and unbalanced heat load (last two considering the developed controllers integrated / dual SISO, SISO and SIMO strategies) were developed and a short description is presented below. More details regarding the development of the controllers can be found in [9]. The results presented are for the LP cycle, but the authors highlighted that similar results were obtained with the VC cycle.

A. *Flow distribution for unbalanced heat loads*

The experimental results showed that for different heat loads applied on the parallel ME's an unbalanced flow exists, which generated a higher temperature on the pseudo chip with higher heat load. Temperatures of 75 °C against 60 °C were obtained when the difference in heat load was 60 W (90 W on ME1 against 30 W on ME2, respectively, emulating the maximum and idle clock speeds of real microprocessors). Despite this, it is important to mention that the temperatures obtained were lower than the typical CPU operating limit of 85 °C and that the difference of temperatures was reduced when the set point of the outlet vapor quality was reduced from 22% to 15% (viz. Figures 3 and 4). As can be seen, a total of eight different combinations of heat loads and three outlet vapor qualities were evaluated.

Regarding the controllability, the cooling systems were found to be fast and effective, controlling the condensing pressure or the secondary fluid temperature (more details in [9]) and the outlet vapor quality at the defined set points under steady state and transient conditions of heat load, and hence indirectly the chip temperature.

B. *Heat load disturbance rejection tests*

The heat loads on ME1 and ME2 were varied between 90 W and 75 W and 75 W and 60 W, respectively, with a periodic disturbance time of 1.4 s (emulating a fast and periodic change in the pseudo-microprocessors' clock speed). Figure 5 shows the input power disturbance on the pseudo chips and the effect on the average temperature of each chip. The maximum temperature variation is only 1.5 °C, which is acceptable when compared to the temperature gradient along the chip for on-chip single-phase cooling using water (about 2-3 K for a uniform heat flux and without heat load disturbance [10]).

Figure 6 shows the controller's reaction under the situation of a disturbance. It can be seen that the SMV controller was able to maintain the exit vapor quality to within ±5% of the set point. What is important to observe is that the controller was effective, i.e. it showed fast response for the induced disturbance and no instability was observed.

Finally, it can be highlighted that the control strategies adopted (SISO, dual SISO and SIMO) were simple but still effective for controlling the specific variables while maintaining the pseudo chips within a safe operating range. In fact, this is done without a temperature signal from the chip, which is very convenient because of the limited bandwidth available on actual CPUs.

Energy in	LP cycle	VC cycle
Pump or compressor input power, W	17.4	102.1
Input power on the pseudo chips, W	164.5	164.5
Input power on the post heater, W	0	125.6
Energy out	**LP cycle**	**VC cycle**
Heat transfer in the condenser, W	68.3	194.2
Energy recovery efficiency %	37.5	49.4
Thermodynamic conditions in the condenser		
Condensing temperature, ˚C	60.0	80.5
Outlet water temperature, ˚C	49.3	65.0

TABLE 1: Energetic analysis for the VC and LP cooling systems and thermodynamic conditions in the condenser.

C. *Energy comparison*

To compare the performance of the liquid pumping and vapor compression cooling systems, which were experimentally evaluated and analyzed beforehand, a steady state condition was selected from the flow distribution tests.

Table 1 shows the results for the power consumption of the drivers, the two systems' input and output energies associated with components and piping, and the thermodynamic conditions in the condenser for the main and secondary working fluids. The experimental condition selected for the comparison was that the input powers on pseudo chips 1 and 2 were 90 W (41.7 Wcm^{-2}) and 75 W (34.7 Wcm^{-2}), respectively.

The results show a higher driver input power for the VC system, about six times, which naturally is associated with the energy expended to lift the pressure from the ME's to the condenser. If one compares the results with a hypothetical air cooling system, considering a COP of 1.22 (45% of the total energy consumption for air cooling system [11, 12]), the energy consumption would be 134.8 W versus 17.4 W when compared with the LP cycle and 237.8 W versus 102.1 W when compared with the VC cycle. This represents a reduction of 87% and 57% in energy consumption, respectively. The differences in air cooling system energy consumption are due to the input power on the post heater (which emulates the heat load of auxiliary electronics of servers, i.e. memories, DC/DC converters, etc.), which was only considered for the VC cycle (*viz.* Table 1). A pump or compressor optimized for this application would consume much less than 17.4 W and 102.1 W, probably less than one-half.

It can also be seen that 50.6% and 62.5% of the energy out of the VC and LP systems, respectively, are associated with heat losses. It shows that improvements can be done to improve the overall performance of the system, which would mainly be associated with the reduction of the driver and piping losses and, consequently, to increase the energy recovered in the condenser. The test bench here is a "plug-and-play" unit designed for versatile testing of components and flow control, not an optimized compact system.

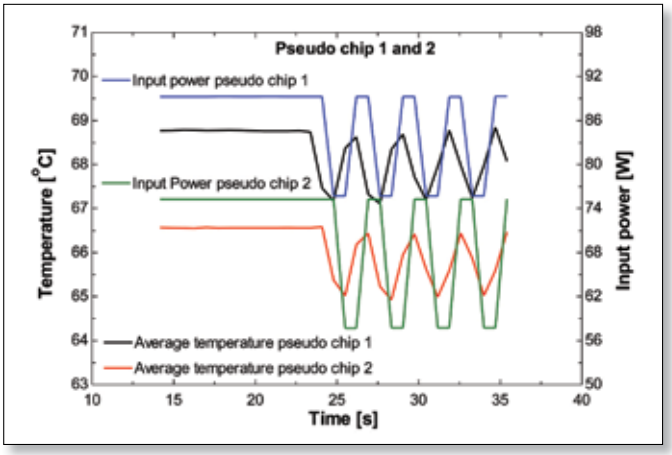


FIGURE 5: Heat load disturbance and pseudo chip temperatures.

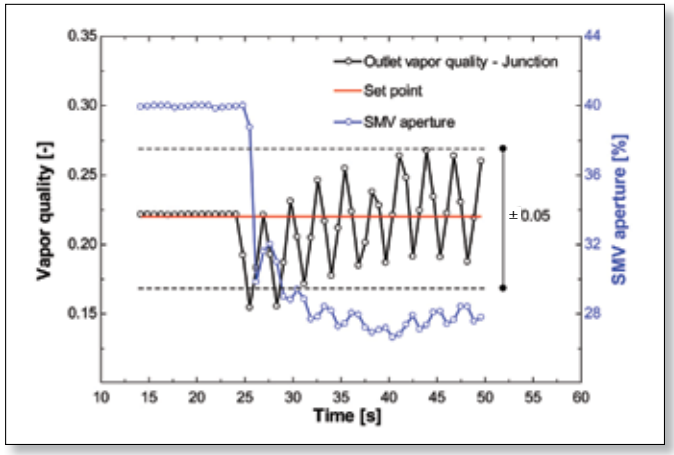


FIGURE 6: Outlet vapor quality and SMV controller.

The results showed a much higher temperature for the secondary fluid at the outlet of the condenser when using the VC system, which is related to the higher condensing temperature. This implies that a higher economic value is obtained for the waste heat available in the condenser. In Europe in particular, many cities have district heat lines (even the small city of Lausanne) and they are potential consumers for the waste heat.

CONCLUSIONS

The present study has demonstrated that simple control schemes are sufficient for management of two-phase on-chip cooling systems for servers, that the cooling is very effective and rapidly responds to step changes in heat dissipation rates, and that this technology provides a low energy consumption relative to air-cooling.

ACKNOWLEDGEMENTS

Wolverine Tube Inc. (Huntsville, AL) provided MicroCool cold plates to our specification while Embraco (Joinville, Brazil) provided the linear oil-free mini-compressor.

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