MEASURED THERMAL RESISTANCE OF MICROBUMPS IN 3D CHIP STACKS

Electronics COOLING

MARCH 2013

BENEFITS AND DRAWBACKS OF USING TWO-PHASE COOLING TECHNOLOGIES IN MILITARY PLATFORMS

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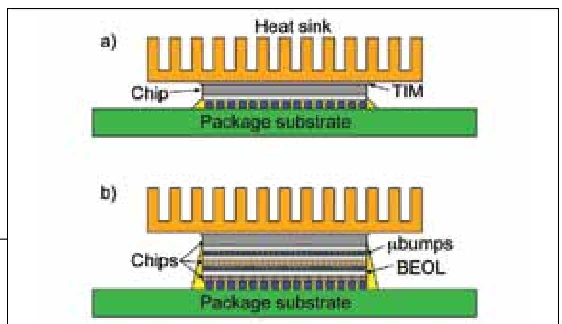

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Editorial

Analysis by the pound

Jim Wilson, Editor-in-Chief, March 2013

With apologies to the SI unit system, price per pound is still a common expression in the US. Consumers know that their costs will scale with the quantity, or pounds, of something they are purchasing. In case you are wondering how this relates to electronics cooling, the analogy is described below. A frequent arrangement in larger companies is having a group of thermal analysts that support multiple projects. The obvious benefits of a common group of analysts are knowledge transfer and mentoring, and as a result, the engineers in this group become specialized and efficient. Company projects obtain thermal design and analysis from the specialized group and pay for this service on a per hour of labor basis. Over time, assuming similarity between projects, reasonable budgets for thermal design and analysis can be estimated. The end result is projects having control of an allocation of engineering hours and the project management purchases thermal design and analysis by the pound from the analysis group.

While the working relationship between project managers and the thermal design engineers (whose services are bought by the pound and are readers of *Electronics Cooling*) has desirable features, conflicts can arise. The thermal design task may be more complex than anticipated or more typically, the design iterations involving interaction with other disciplines takes longer to converge. While the analysts should be in the best position to judge how much effort is needed, the managers have a responsibility to keep the project within the financial constraints and as expected, they do not buy any more pounds of analysis than they judge is needed or can be afforded. Examples exist at both extremes of finding the right balance of analysis needs. Most of us know of someone who simply has to be told to stop refining their computational models. A manager applying a budget constraint is doing them a favor by pointing out the diminishing returns of the effort. The opposite case is the project that decided it would save money by foregoing analysis but soon regrets the decision when parts overheat in testing. Buying fewer pounds of design and analysis than is really needed may appear to be cost effective in the short term but detrimental in the longer term.

One other drawback to the bought by the pound system related to thermal design and analysis is the lack of thermal ownership from the analysts. When they only interact with a project to build and solve a model and then move on, both the projects and analysts suffer. This is especially true with complex systems that take a long time to design. The programs can suffer because there is not someone keeping watch over the thermal performance. A typical example is the transition of a design to a lower cost and easier to produce design but the team doing this task may forget to consider the thermal implications. The analysts lose out on the experience of seeing how the product is really built and how it performs. My advice to the thermal analysts is to make an effort to stay involved and gain experience at all levels of product design, manufacture, and test. This experience helps in tailoring thermal design and analysis tasks such that you can provide the best answer within the budget and schedule limits. Similarly, I encourage managers to recognize the long term benefits of continuing interaction between thermal analysis and projects.

As a closing note, Clemens Lasance informed us in his last editorial column that he is stepping down from the responsibility of editor in charge of an issue. I would like to personally thank him for his many contributions to the field of electronics thermal management and for shaping ElectronicsCooling into the valuable resource that it is today. Clemens was not afraid to challenge the practice of doing things the way we always have and advocated fully understanding the underlying principles of thermal management. Even in discussions over the technical relevance and value of potential articles we jointly reviewed over the past years, I have appreciated his consistency of never wanting to provide anything but the most educational and technically sound viewpoint to our readers. I wish him pounds of success as he weighs in on other efforts.

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Cooling Matters

Applications of thermal management technologies

NEW COOLING METHOD BASED ON MILITARY FIGHTER JET AIR FLOW TECHNOLOGY

Engineers at GE Global Research have unveiled a new method of moving air in order to cool consumer electronics based on technology used to improve air flow in military fighter jets. Tentatively known as a "dual piezoelectric cooling jet," the technology consumes an average of 50 percent less energy than modern fan-powered cooling units.

The dual piezoelectric cooling jets consists of two thin nickel-based discs connected by special ceramics. When the ceramics are triggered with an AC signal, the metal discs are activated and begin to "pump" air. According to GE's report, the metal discs are currently capable of expanding as fast as 150 times per second.

General Electric has announced a partnership with semiconductor company Texas Instruments to put the company's dual piezoelectric cooling jet technology on the market by the end of this year.

Source: Forbes

RESEARCHERS EXAMINE HEAT DISSIPATION IN 3D INTEGRATED CIRCUITS

A team of UT Arlington researchers funded by the National Science Foundation has been formed to examine potential solutions for heat minimization and dissipation in three-dimensional integrated circuits.

According to Ankur Jain, assistant professor of mechanical and aerospace engineering at UT Arlington and a member of the research team, the limited amount of available space on an integrated circuits has forced engineers to "build vertically, placing wafers on top of wafers."

Though the use of three-dimensional integrated circuits has improved performance and efficiency, the heat generated by the design has become a problem.

The research team plans to investigate fundamental thermal transport at UT Arlington and examine through-silicon vias (TSVs) as part of their research.

Source: AZ Nano

WIND TUNNEL-COOLED COMPUTER MAY HELP CURE CANCER

Blogger Mike Schropp of "Total Geekdom" recently revealed the construction of his new wind tunnel-cooled computer. Designed for grid computing, Schropp's new computer is part of IBM's World Community Grid, which combines a worldwide network of computers into a supercomputer that is working to identify cures for cancer and AIDS and find solutions to other areas of medical and humanitarian research.

Schropp constructed the basic shape of the wind tunnel out of MDF board composite, angle aluminum and polycarbonate, and installed a series of lever switches to control both the fan and the power to the LED temperature gauges. A standard box fan was placed at the air intake section of the wind tunnel.

The wind tunnel-cooled computer is currently processing 8,000 single workunits per day, approximately 20 times the capability of a standard IBM World Community Grid member.

Source: Total Geekdom

Datebook

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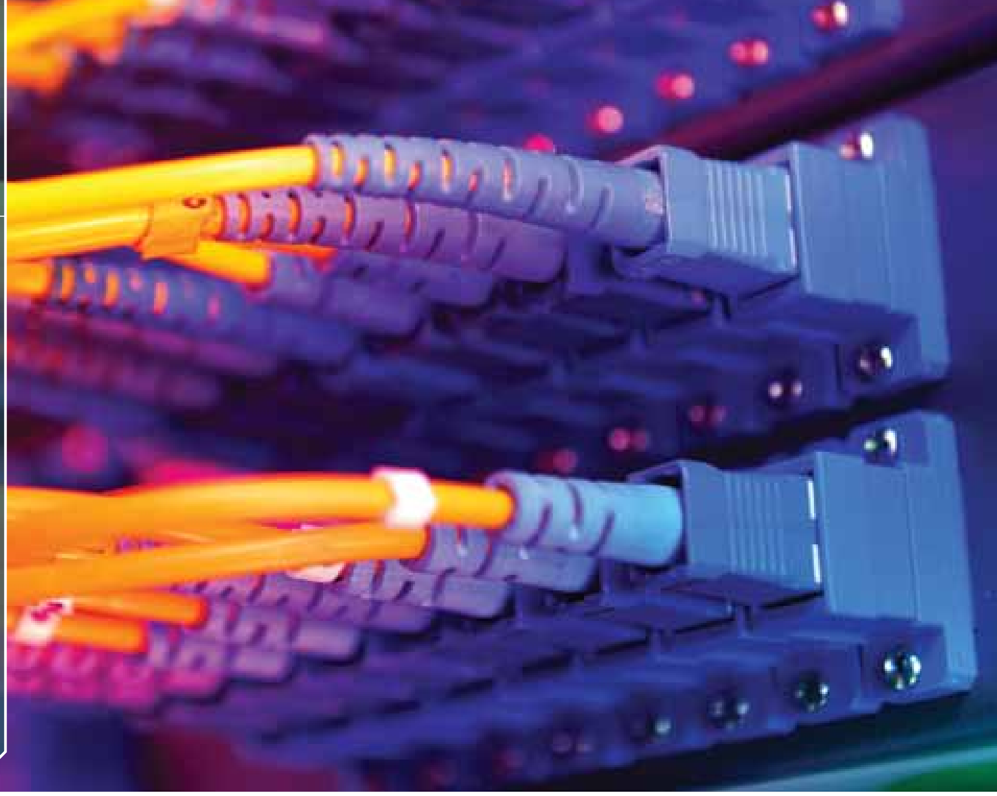
EUROPEAN COMMISSION: ACTION ON RAISING DATA CENTER TEMPERATURES

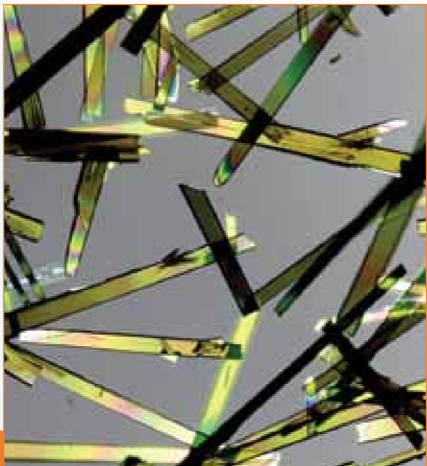
The European Commission has asked the IT industry for faster, more decisive action on the issue of raising data center temperatures to enable more free air cooling.

There are still a large amount of data centers with a low cooling set point and narrow humidity control that rely on power-hungry mechanical chillers. A report published by data center efficiency advocate The Green Grid states the current beliefs regarding data center equipment's tolerance to heat and humidity are based on outdated practices dating back to the 1950s and the majority of data centers have yet to make the adjustments.

Source: Tech World



RESEARCH SUGGESTS FERROELECTRIC CRYSTALS MAY ASSIST WITH COMPUTER CHIP HEAT REGULATION



Researchers at the Carnegie Institution in Washington, D.C. have discovered a new, efficient way to extract heat using ferroelectric crystals. The crystal materials exhibit an electrical polarization in the absence of an electrical field that can be reversed by applying an external electrical field, resulting in a significant temperature change.

Ronald Cohen, staff scientist at Carnegie's Geophysical Laboratory and University of Chicago student Maimon Rose performed atomic-scale molecular dynamics simulations on the ferroelectric crystals. According to Cohen, the application of an external electrical field allows the crystals to assist with extracting heat. He adds that "the effect is larger if the ambient temperature is well above the transition temperature, so low transition temperature materials are preferred.

The researchers hope to use the crystals on computer chips to assist with current overheating and meltdown issues and remove the limit on higher computer speeds.

Source: The Carnegie Institution for Science

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Are Critical Heat Fluxes of LEDs And ICs Comparable?

Clemens J.M. Lasance, Guest editor

FACT: MANY PAPERS discussing LED thermal management issues report values of about 100 W/cm2 and use the same arguments as are valid for ICS to demonstrate that some critical value has been reached. The question to be addressed: is this indeed a fact or can it be shown to be a fairy tale, and hence do we need different arguments to judge LEDs and ICs?

Let us start with a convincing example. Suppose we compare the two following cases for liquid cooling:

They differ only in the source and spreader areas, keeping the heat flux constant.

The next table shows the results for both the average and maximum temperature of the sources.

The values are calculated using the heat spreader equations derived by Song, Lee and Au [1].

What do the results tell us? Two significant facts.

Firstly, the larger the source, the larger the temperature difference between the average and the maximum temperature (this is, by the way, an important drawback of the very useful web-based calculator by the U. of Waterloo [2] that only presents the average temperature over the source). The problem is caused by the fact that we are dealing with increasing temperature gradients over the surface when the area increases with respect to the source.

Secondly, the maximum temperature of the smaller source with the same heat flux results in a temperature drop of more than a factor of 5. How these values are related can best be observed by taking a look at the L-equation [3,4,5] that can be used over a quite large range of practical applications but is not as accurate as the SLA-equations:

$$(1)\quad R_{thj} = \frac{1}{hA_{spreader}} + \frac{\ln\left(\frac{\text{--}spreader}{A_{source}}\right)}{4\pi kd} - \frac{y}{2\pi kd}$$

The first term can be considered a convection term, the second a conduction term and the third a correction term. It is easy to see why the temperature goes down when the area ratio is kept constant. Only the first term changes, and in our case the conduction term is much larger than the convection term for the larger source (indicates negligible heat spreading), and much smaller for the smaller source (indicates significant heat spreading). Simply put: the heat fluxes do not scale when only the areas are changed while keeping the area ratio constant. In order to scale correctly, the product k*d should also be scaled, meaning in this case that the thickness should be reduced by a factor of 100 for the smaller source to result in the same temperature rise keeping the flux constant. Because this is never the case in practice due to the fact that the PCB or submount is more or less fixed, we cannot compare critical heat fluxes without mentioning at least the source area. In closing this example, let us compare the critical heat flux that corresponds with a maximum temperature rise of 60 °C for both cases.

The big difference is noteworthy, and boils down to the following: what is called a critical heat flux for ICs is not per se critical for LEDs.

You may wonder why people always talk W/cm2. The reason is that the thermal management field has been dominated by the cooling of processors that have dissipating areas of order (cm^2).

How to prevent these misunderstandings? First, designers should be aware of the problem. A useful rule of thumb has been formulated by Wilcoxon and Cornelius [6] using the following equation showing the relation between a critical flux and the source area:

$$(1)\quad q = \frac{300}{\sqrt{A}}\ ,\ q\ in\ W/cm^2,\ A\ in\ cm^2$$

Its use is limited to areas larger than about 0.1*0.1 mm2 being only a problem

	Area Source	Area Spreader	Thickness d	Thermal cond. k	h	power	flux
	cm^2	cm^2	mm	w/mk	w/m^2k	w	w/cm^2
A	1	10	1.6	160	10000	100	100
B	0.01	0.1	1.6	160	10000	1	100

for applications involving very small sources. It should also be realized that this limit is only a very rough estimate and depends not only on the source size but also on the spreader thickness, area, thermal conductivity and boundary conditions.

What every designer should do who is being confronted with heat spreading is to use spreadsheet software with the SLA equations, in such a way that h and k are considered parameters. It is then easy to get enough data in a couple of minutes to construct useful graphs.

CONCLUSION

It is important to understand that it does not make sense to use the same heat flux limits for both processors and LEDs alike, and I propose to authors dealing with high-power LED applications to refrain from mentioning e.g. $100 W/cm^2$ as a critical value above which liquid cooling should be used, based on IC-related data. Instead, I suggest to quote the 'raw' data related to the size of the source, e.g. for a junction W/µm2, for an LED W/mm^2, for a die W/cm^2, for a TV backplane or a large LED luminary W/m^2.

	ΔT average	ΔT maximum
Source 1 cm^2	53.8	68.9
Source 1 mm^2	13.4	14.4

	Critical heat flux for $\Delta T_{max} = 60^{\circ}C$ W/cm^2
Source 1 cm^2	417
Source 1 mm^2	78

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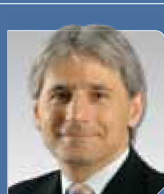
Understanding the Thermoreflectance Coefficient for High Resolution Thermal Imaging of Microelectronic Devices

Kazuaki Yazawa, Microsanj/Purdue Univ., **Dustin Kendig,** Microsanj,
Peter E. Raad, TMX Scientific/SMU, **Pavel L. Komarov,** SMU, **Ali Shakouri,** Purdue Univ.

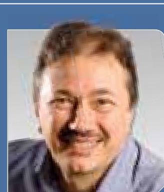
Kazuaki Yazawa received a PhD from Toyama Prefectural University in Japan and has more than 29 years of experience in thermal management of electronics as a distinguished engineer at Sony Corporation. After leaving the company, he also worked on thermal imaging research along with thermoelectric energy conversion devices/systems at University of California Santa Cruz for two-and-a-half years and is continuing research at Purdue University on the topics criticized in Microsanj from various industrial needs.

Dustin Kendig is vice president of engineering at Microsanj, LLC. He received a B.S. with honors in electrical engineering from University of California Santa Cruz with research focused on device characterization using thermoreflectance imaging where he studied microscopic defects in photovoltaics, heating in power transistor arrays and thermoelectric materials.

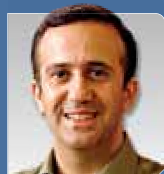
Peter E. Raad is currently a full professor of mechanical engineering at SMU and holds the Linda Wertheimer Hart Professorship. In 2006, he founded TMX Scientific to commercialize novel submicron thermal metrology systems. He has received several teaching and research awards, including the ASME North Texas Section Engineer of the Year in 1999-2000, and the Harvey Rosten Award for Excellence in 2006. He received his Ph.D. in mechanical engineering from the University of Tennessee at Knoxville in 1986. He has published more than 50 articles and given more than 100 conference and invited talks. He is a Fellow of ASME and Senior Member of IEEE.



Pavel L. Komarov is currently a research professor at SMU. He joined the Nanoscale Electro-Thermal Sciences Laboratory at SMU in 1997, where he has been a lead designer and developer of experimental and numerical tools for the thermal measurements of thin- film materials and micro-electronic devices. He received the Ph.D. in physics and mathematics from the Institute for High Temperatures of the Russian Academy of Sciences in 1996. He has published more than 45 articles, and in 2006 received the Harvey Rosten Award for Excellence.



Ali Shakouri is the Mary Jo and Robert L. Kirk director of the Birck Nanotechnology Center and a professor of electrical and computer engineering at Purdue University. He received his engineering degree from Telecom Paris, France in 1990 and Ph.D. from California Institute of Technology in 1995. His current research is on nanoscale heat and current transport in semiconductor devices, high resolution thermal imaging, micro refrigerators on a chip, and waste heat recovery systems. He received the Packard Fellowship in 1999, the NSF Career award in 2000 and the UC Santa Cruz School of Engineering FIRST Professor Award in 2004.



INTRODUCTION

THERMOREFLECTANCE thermal imaging is an optical technique for measuring, with external illumination, the relative change in the surface reflectivity as a function of temperature for a specific sample or semiconductor device. As the temperature of the sample changes, the refractive index, and therefore, the reflectivity also changes. A first order relationship between the change in reflectivity and the change in temperature can be approximated as [1,2]

$$\frac{\Delta R}{R} = \left(\frac{1}{R} \frac{\partial R}{\partial T} \right) \Delta T = \kappa \Delta T$$

where, κ is the ***Thermoreflectance Coefficient***

The Thermoreflectance Coefficient is a basic material property that depends on illumination wavelength, ambient temperature, microscope numerical aperture, material surface characteristics and, in some cases, may have some dependence on the material processing technique. For most metals and semiconductor materials of interest, the value of the Thermoreflectance Coefficient will be in the order of 10^{-2}/K to 10^{-5}/K. Thus, to detect a temperature change of 1 °C, it is necessary to detect a reflectance change of 1 part in 100 to 1 part in 100,000. It is important therefore, to pre-obtain an accurate value for the Thermoreflectance Coefficient to achieve the best temperature resolution when doing thermal analysis on semiconductor devices. It is equally

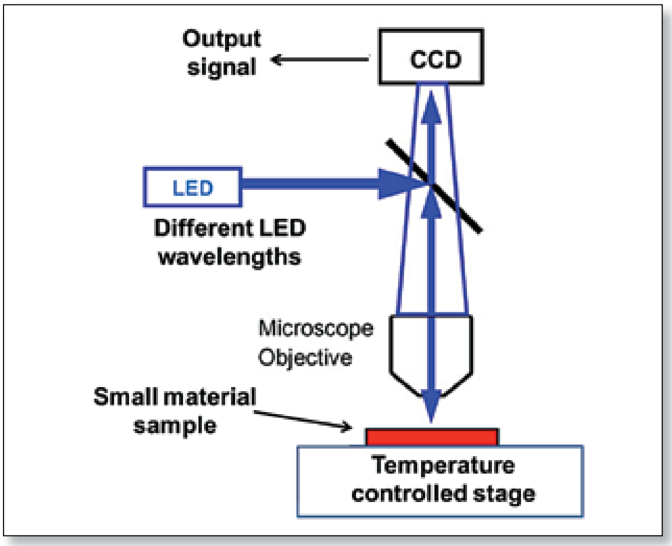


FIGURE 1: Determining the Thermoreflectance Coefficient.

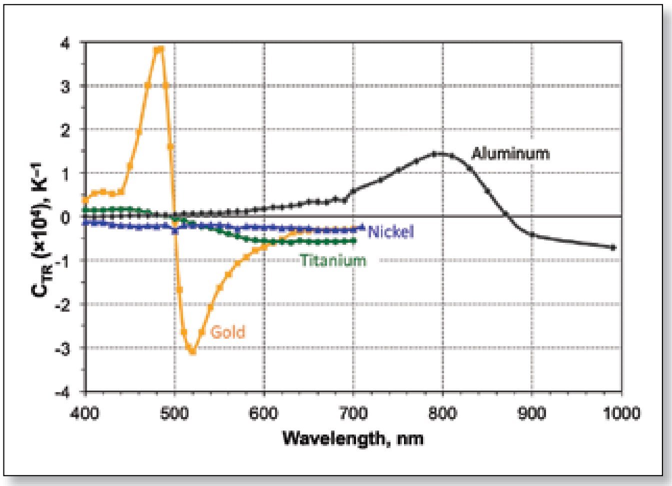


FIGURE 2: Thermoreflectance coefficient vs. illumination wavelength for various materials (Raad et al. [3])

important to select an illumination wavelength that provides a Thermoreflectance Coefficient to be near the maximum value for the material being analyzed. The illumination wavelength also impacts the spatial resolution so, in some cases, a tradeoff may be warranted to achieve the desired results.

The purpose of this paper is to provide a better understanding of how κ, the Thermoreflectance Coefficient, varies with respect to:

- Material Temperature
- Device Material Properties
- Illumination Wavelength
- Optics/Microscope Numerical Aperture

MATERIAL TEMPERATURE

Compared to IR thermography, the thermoreflectance technique has the important advantage of working over a very wide temperature range. The Thermoreflectance Coefficient does have a dependence on the material temperature, but fortunately, this dependence is relatively small. As an example, the thermal performance of copper micro-vias, only a 2.7 % change in Thermoreflectance Coefficient was detected for a temperature change of approximately 200 °C. Additionally, good thermal images of gold contact layers in small devices have been obtained with sub-micron spatial resolution over temperatures ranging from 10 K to 800 K. Obviously, if the best possible precision is required, it is necessary to measure the Thermoreflectance Coefficient at operating temperatures of interest.

MATERIAL PROPERTIES

Processing Technique: For any given material, the Thermoreflectance Coefficient is not a strong function of surface preparation or the deposition process. Calibration for each device under test therefore, is generally not required. This differs from IR thermography where the emissivity can change substantially and as a result, must be calibrated each time to obtain accurate temperature data. The Thermoreflectance Coefficient of gold prepared by various thermal or e-beam evaporation techniques was measured and always showed consistent values. On the other hand, if there is a significant difference in the visual color of the material due to major microstructures, porosity variations, or surface oxidation, the Thermoreflectance Coefficient can be affected significantly.

Dielectric Coatings and Passivation Layers: Dielectric coatings or passivation layers will change the reflective properties and thus the Thermoreflectance Coefficient. Due to optical interference in thin layers, oscillations in the thermoreflectance signal can be observed. For these cases, if there are adjacent coated and uncoated regions on the sample, one can use temperature continuity on the surface to calibrate the thermoreflectance coefficient. If this is not feasible, the Thermoreflectance Coefficient needs to be determined. This can be done by mounting a sample with small thermal mass on a temperature-controlled stage and measuring the change in reflected signal versus temperature (Fig. 1).

Multiple temperature cycles and averaging are necessary to obtain good signal to noise ratio. Conducting the experiment with different illumination wavelengths simplifies the analysis as optical interference peaks are shifted and one could use the envelope of the measured signal to extract the temperature profile.

Material	470 nm (Blue)	530 nm (Green)	585 nm (Yellow)	660 nm (Red)	780 nm (Near-IR)	1050-1300 nm
Gold (Au)	•	•				
Aluminum (Al)					•	
Nickel (Ni)			•	•		
Titanium (Ti)			•	•		
Silicon (Si)	•					
Gallium Arsenide (GaAs)	•					
Indium Phosphide (InP)	•					
Thru-the-Substrate Imaging						•

TABLE 1: Recommendation of illuminating wavelengths for various materials.

ILLUMINATION WAVELENGTH

For any particular material, the Thermoreflectance Coefficient is very strongly dependent on the illumination wavelength. As illustrated in Fig. 2 [ ], the Thermoreflectance Coefficient for aluminum is near zero at an illumination wave-

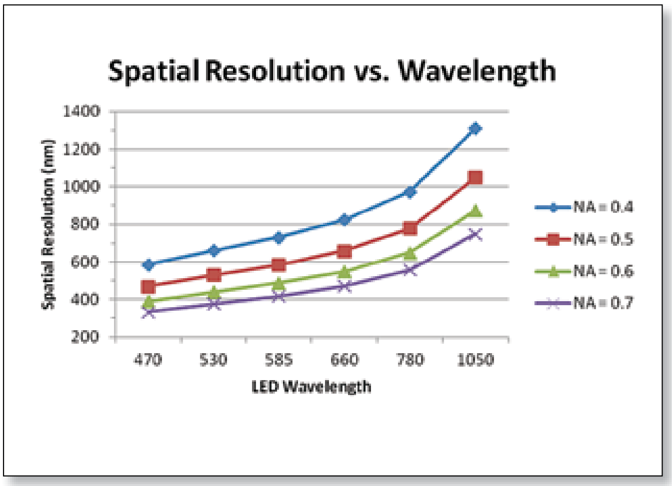


FIGURE 3: Spatial Resolution vs LED Wavelength.

length of 400 nm and orders of magnitude higher at 800 nm. In the case of gold, the Thermoreflectance Coefficient has a positive peak value at about 470 nm, goes to zero at about 500 nm, and exhibits a negative peak value at about 520 nm. It is therefore, very important to select the appropriate illumination wavelength for the materials being analyzed.

The following table lists the recommended LED wavelength for typical materials to obtain near optimal values of the Thermoreflectance Coefficient. Note that two alternatives are shown for gold, one for the positive peak and one for the negative peak. Two sources are also indicated for Nickel and Titanium since the peak values for both of these materials are quite broad.

For other material systems, one can easily extract the Thermoreflectance Coefficient if there is an embedded temperature sensor on the chip near the region of interest. The calibration procedure entails heating the entire chip uniformly using an external thermal stage. The thermoreflectance change across the full sample is recorded by the CCD while the temperature is measured simultaneously with the sensor. The calibration image and sensor measurements are correlated to produce values for the Thermoreflectance Coefficient for each region-of-interest on the chip.

In the absence of a temperature sensor, the Thermoreflectance Coefficient can be determined in the manner described earlier, using a sample of the chip with a small thermal mass (e.g. 1x1 mm^2 up to 1x1 cm^2 die) so that the temperature can be cycled.

MICROSCOPE OBJECTIVE NUMERICAL APERTURE (NA):

The magnitude of the Thermoreflectance Coefficient also has a dependence on the numerical aperture of the microscope objective used in the imaging [9]. This is due to the component of the light polarized perpendicular to the surface which can be non-negligible for high numerical apertures, e.g. NA > 0.5. The spatial resolution is known to be determined by the following expression:

Spatial Resolution = $\lambda/[2 \cdot n \cdot \mathrm{Sin}(\theta)]$

where λ is the wavelength of the illumination source, n is the index of refraction (1.0 for air), and θ is the half-angle of the cone of light exiting the microscope lens. The component n·sin(θ) is called the Numerical Aperture (NA) and is dependent on the optics and objectives of the microscope.

The above relationship is shown in Fig. 3 for wavelengths up to the near infrared (NIR) range.

For precise measurements of temperature distribution with a high NA lens, it is recommended to:

a) Perform measurements initially with a low NA and low magnification lens over a large area and

b) Without changing anything in the device, change the lens to higher NA and scale the temperature data accordingly.

This approach works when relatively large areas of the sample surface are available for imaging (e.g. 50-100 microns diameter). If the region of interest is very small and only visible with a high NA lens, then direct calibration on a temperature-controlled stage is necessary. Since small changes in the stage temperature can defocus the image seen by a high NA lens due to the thermal expansion of the sample, autofocusing during calibration is required.

SUMMARY

Having an accurate Thermoreflectance Coefficient and selecting the right illumination wavelength are key steps for achieving the best thermal and spatial resolutions for thermoreflectance thermal imaging of microelectronic devices. For unique materials and devices without embedded temperature sensors, the Thermoreflectance Coefficient is determined with a small sample of the material on a temperature-controlled stage.

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Application of Transient Thermal Methods to Moisture Diffusion Calculations, Part 2

Bruce Guenin, Assoc. Editor

INTRODUCTION

THIS TWO-PART column was motivated by concerns regarding the important role of organic materials in electronic systems and their accompanying vulnerabilities due to moisture diffusion. The methods described herein are intended to provide an efficient means of predicting the rate of moisture diffusion under a variety of conditions in order to better manage the associated risks.

Part 1 established the basic validity of the methodology and demonstrated its use in modeling 1-D (one-dimensional) diffusion flow geometries[1]. Part 2 continues the development of these methods and applies them to a variety of situations of practical importance.

CALCULATION METHOD FOR 2-D DIFFUSION GEOMETRIES

As demonstrated in Part 1, the use of a multi-stage RC (resistor-capacitor) network, solved using a numerical method, can be extended beyond its original scope involving thermal transient modeling to the prediction of moisture diffusion. It can be adapted to various geometries by using the appropriate analytical formulas for calculating the particular values of R and C. The execution of the numerical method is relatively independent of these geometrical details.

Figure 1 depicts the geometry assumed in the calculation, that is representative of the design of organic laminates used in package substrates and PCBs (printed circuit boards). It represents a single dielectric core region in a muli-layer package substrate. The core material is the same as that in Part 1, namely, BT ((bismaleimide triazine). The BT is assumed to be 0.015 cm thick and is 1 cm square. It is assumed to be sandwiched between two continuous copper planes. The presence of the copper is not explicitly accounted for in the model. Their effect, as far as the model is concerned, is to prevent any diffusion of moisture into the BT from its top and bottom surfaces. Moisture can only diffuse into the core by way of the exposed edge. Note that this is a a very simplifying assumption. To the extent that the metal planes prevent the diffusion of moisture from one core to another, it is only necessary to model a single core to capture the physics of the diffusion process.

However, in the real world, life is not quite this simple. Typically, in laminated organic package substrates and PCBs, there are perforations in the metal planes as required by the fabrication process or resulting from via or trace routing in the laminate. These perforations would serve to provide additional paths for moisture to diffuse into the interior regions of the laminate. Hence, the time for moisture diffusion in actual components would tend to be less than that predicted here. However, the simple construction assumed here will enable us to more efficiently explore the basic physical effects involved with the exchange of moisture between an organic substrate and the ambient air and simultaneous diffusion within the component.

Before the numerical method can be applied, it is necessary to subdivide the sample into several regions, each of which must be represented by a separate value of R and C in the RC circuit. There is no standard way to do this. However, the method used in Part 1 for a 1-D flow in a slab-shaped component can be adapted to the 2-D situation as follows:

- Circularize the square by transforming it into a disk having an equal area. This has been shown to be a reasonable approximation for radial heat flow in a square geometry[2].
- To create the capacitor volumes, divide the disk into 4 annular regions for which $r_{OUT} - r_{IN} = r_{DISK}/4$, where

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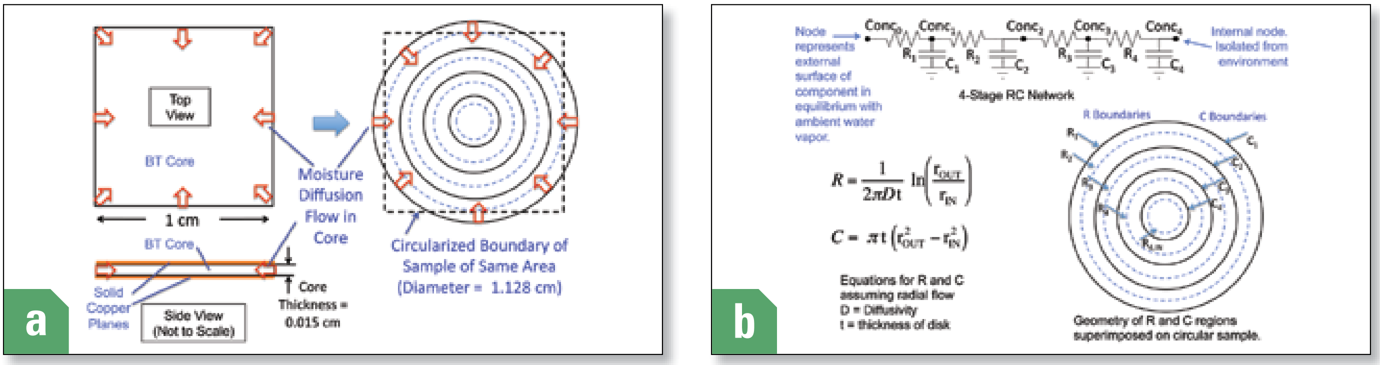

FIGURE 1: a) Diagram of diffusion sample **b)** 4-stage transient RC circuit representing the diffusion process. Diagram of boundaries for capacitor regions (solid lines) and resistor regions (dotted lines). Equations shown, for calculating R and C values, representing 2-D diffusion.

TABLE 1: CALCULATED VALUES OF R AND C

CIRCUIT ELEMENT	MAT'L	INNER RADIUS	OUTER RADIUS	THICKNESS	TEMPERA-TURE	D	R	C
		(cm)	(cm)	(cm)	(°C)	cm^2/sec	(sec/gm)	cm^3
R1	BT	0.499	0.564	0.015	60	1.29E-08	1.01E+08	
R2	BT	0.360	0.499	0.015	60	1.29E-08	2.69E+08	
R3	BT	0.223	0.360	0.015	60	1.29E-08	3.93E+08	
R4	BT	0.100	0.223	0.015	60	1.29E-08	6.62E+08	
R1	BT	0.499	0.564	0.015	85	3.03E-08	4.32E+07	
R2	BT	0.360	0.499	0.015	85	3.03E-08	1.14E+08	
R3	BT	0.223	0.360	0.015	85	3.03E-08	1.67E+08	
R4	BT	0.100	0.223	0.015	85	3.03E-08	2.82E+08	
R1	BT	0.499	0.564	0.015	105	9.44E-08	1.39E+07	
R2	BT	0.360	0.499	0.015	105	9.44E-08	3.67E+07	
R3	BT	0.223	0.360	0.015	105	9.44E-08	5.37E+07	
R4	BT	0.100	0.223	0.015	105	9.44E-08	9.04E+07	
C1	BT	0.423	0.564	0.015				0.0066
C2	BT	0.282	0.423	0.015				0.0047
C3	BT	0.141	0.282	0.015				0.0028
C4	BT		0.141	0.015				0.0009

r_{OUT} and r_{IN} are the outer and inner radii of a given annulus and r_{DISK} is the radius of the disk. This is depicted by the array of concentric solid-line circles in Figure 1.

- The resistor geometries span two adjacent annuli and terminate at the bisecting radius of each. [The bisecting radius divides each capacitor annulus into two equal areas.] This is depicted by the array of concentric dotted-line circles in Figure 1.
- The C and R values can be calculated using the particular values of r_{OUT} and r_{IN} of the appropriate annuli and the appropriate formula in Figure 1.

Table 1 lists the inner and outer radii for each C and R region, and the resultant C and R values. The R calculations assume three different diffusion coefficients, one for each of the three BT temperatures assumed in the case studies to follow.

ADAPTING DIFFUSION CALCULATION METHOD TO DIFFERENT ENVIRONMENTS

Visually, the most prominent feature of the 4-stage RC circuit is the ladder arrangement of the resistor and capacitor symbols. From a physical perspective, the topology of this network and the particular R and C values will determine how rapidly moisture will be transported through the structure. However, the value of $Conc_0$, the moisture concentration at the outer skin of the BT, is important in providing the potential difference to drive the diffusive flow of moisture either into or out of the BT. The value of $Conc_0$ is, in turn, determined entirely by the local RH at the exposed surface of the BT and by its local temperature.

Hence, in order to accurately predict the instantaneous diffusion rate within the BT, it is necessary to determine:

• The diffusion coefficient — it is determined only by the choice of organic material and its temperature.
• Local RH at the exposed surface of the organic material — determined by the ambient temperature and RH and the local temperature of the material.
• Equilibrium value of $Conc_0$ — determined by the local temperature and local RH and the choice of organic material. The following sections provide procedures for calculating each of these properties and the relevant environmental conditions:

Diffusion Coefficient

In Part 1, a method of calculating D for BT was described using Eqn. 3 (in Part 1), and assuming an activation energy for moisture diffusion of 0.48 eV. Table 2 provides calculated values of D at temperatures of interest. Since D is an exponential function of temperature, its value changes significantly with changes in temperature.

Relative Humidity at Interface with the Sample

The value of RH at the interface with the polymer component plays a significant role in the ultimate moisture concentration in the sample. It is critically dependent on the ambient temperature. In situations in which the substrate temperature differs from that of the ambient, then this difference must be taken into account.

The following equation, which provides the relationship between the partial pressure of water in the atmosphere, at saturation, as a function of temperature, can be used as the basis of all the required relative humidity calculations.

$$(1)\quad P_{Water,Sat}(T) = \frac{e^{(77.3450+0.0057\text{-}7235/T)}}{T^{8.2}}$$

where $P_{Water,\,Sat}$ is the partial pressure of water in units of Pa and T is the absolute temperature, in units of K [3]. At a given value of RH, the partial pressure of water is simply equal to (2)

$$P_{Water}(T,RH) = RH \bullet P_{Water,Sat}(T) = RH \bullet \backslash \frac{e^{(77.3450+0.0057\text{-}7235/T)}}{T^{8.2}}$$

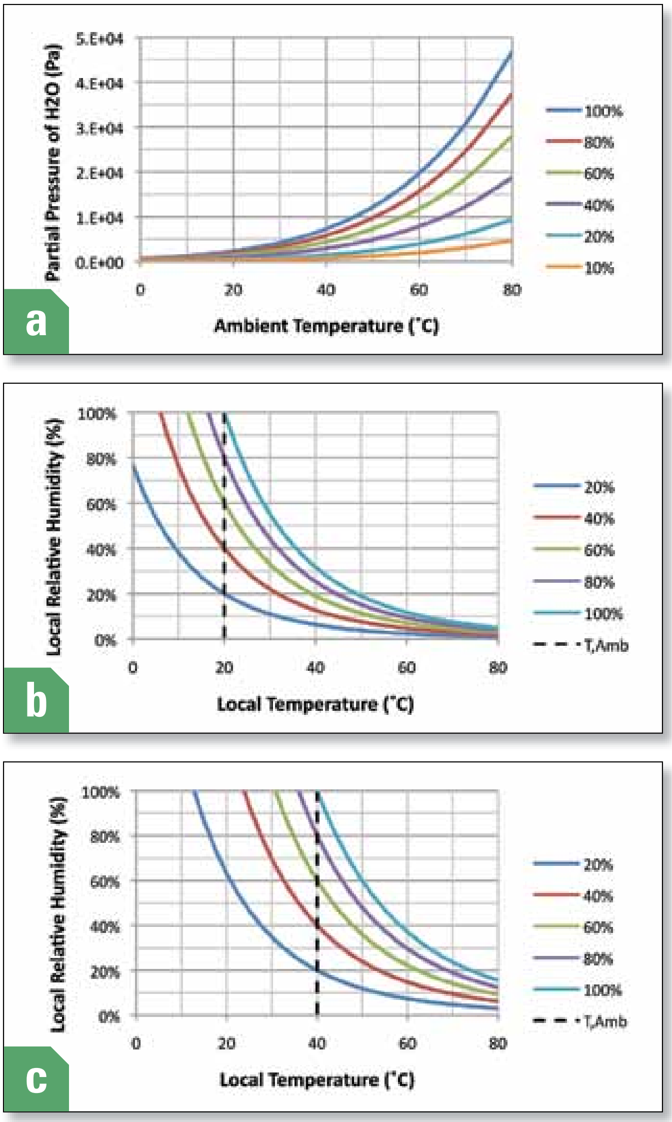

FIGURE 2: a) Graph of H2O partial pressure vs ambient temperature and relative humidity, **b & c)** Local relative humidity at sample surface vs local sample temperature and ambient RH. The ambient temperature was assumed to be fixed: b: 20°C, c: 40°C."

TABLE 2: CALCULATED COEFFICIENT FOR MOISTURE DIFFUSION IN BT

T	D(T)	D(T) D(20)
(°C)	(cm^2/sec)	
20	1.32E-09	1.0
30	2.47E-09	1.9
40	4.44E-09	3.4
50	7.69E-09	5.8
60	1.29E-08	9.8
70	2.10E-08	15.9
80	3.33E-08	25.2
90	5.14E-08	39.0
100	7.75E-08	58.8

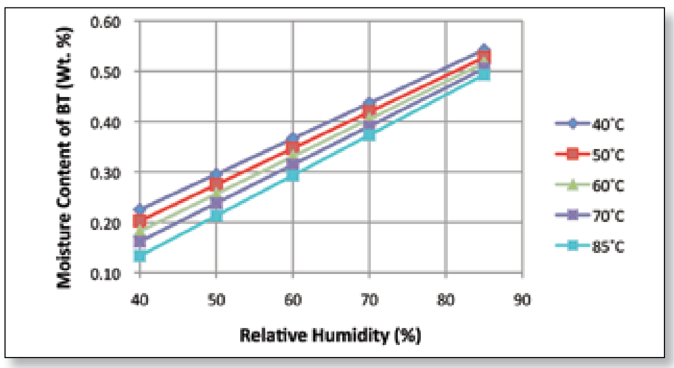

FIGURE 3: Saturated moisture content of BT vs relative humidity and ambient temperature. Regression fit to data in Ref [4].

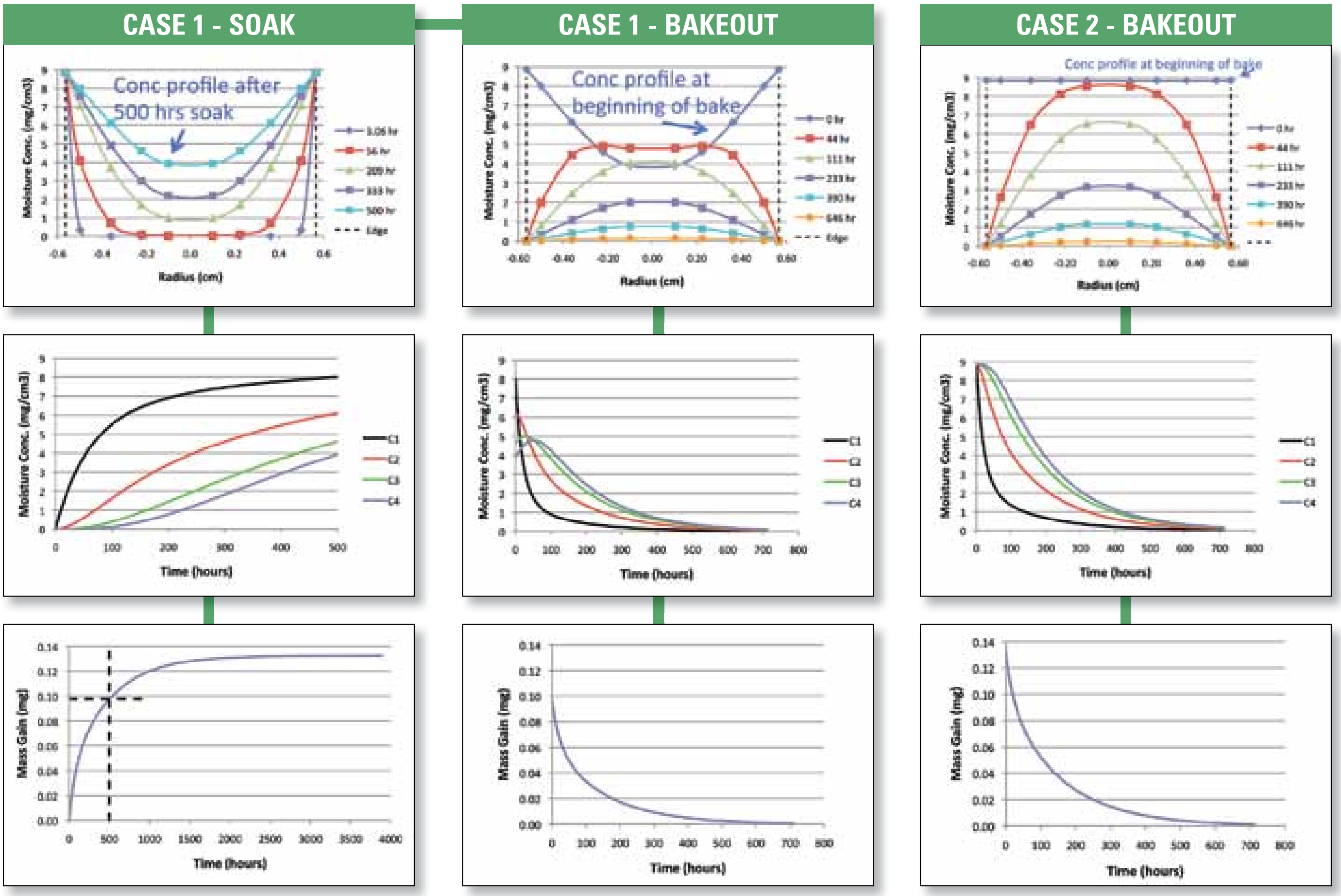

FIGURE 4: Solution results for BT samples, 85˚C/85%RH soak and 105˚C bakeout exposure for Cases 1 and 2: 2-D diffusion profile versus time (top graphs). Concentration values at each capacitor versus time (middle graphs). Mass gain curve versus time (bottom). In Case 1, 500 hour soak did not saturate BT. In Case 2, soak achieved full saturation.

Equation 2 was used to generate the various curves of P_{Water} vs temperature at specified values of RH in Figure 2a. Eqn. 2 was also used to create the curves in Figures 2b and c. Their behavior results from the fact that, when a surface is maintained at a local temperature different from the ambient, the RH value at that surface is also different from the ambient RH. Figure 3b assumes an ambient temperature of 20˚C. When a given surface is heated the partial pressure of the water in the air at its surface is unchanged. However, since the hotter air at the interface has a higher $P_{Water,\ Sat}$, the local RH is reduced compared with the ambient value. Conversely, when a surface is cooled, the RH increases and can lead to condensation (i.e.: the local RH reaches 100%). The graph accounts for that effect also. Figure 3c shows the same sort of curves, but this time, assuming an ambient temperature of 40˚C. The higher value of $P_{Water,\ Sat}$ at a 40˚C ambient leads to higher values of local RH at a given surface temperature than for 20˚C.

Moisture Concentration at the Sample Surface

The relationship between the saturated moisture concentration and ambient temperature and RH for BT samples in equilibrium with the ambient has been quantified though weight measurements on saturated samples [4]. Figure 3 shows the result of applying a regression analysis to the raw data from the reference and provides a means of estimating values of moisture concentration at values of temperature and RH other than those measured. Furthermore, a power law regression (not shown on the graph) was generated for each trendline and was used to estimate values for RH between 0 and 40%.

MOISTURE DIFFUSION CALCULATIONS FOR 6 CASE STUDIES

A total of 6 case studies were performed. They are listed in Table 3. In all cases there was a soak process under 85˚C/85%RH conditions. For Case 1 the soak process lasted for 500 hours, and was simulated explicitly. For all other cases, they were assumed to proceed to saturation. They were not explicitly simulated. Their effect was represented by assigning a constant value of concentration (equal to 8.85 mg/cm3) to all of the capacitors as an initial condition in the bakeout simulation.

Cases 1 and 2 are similar to the one analyzed in Part 1. The simulation results for these cases are shown in Figure 4. In this Figure, the top row of graphs plot the value of moisture concentration calculated for each of the capacitors at various values of elapsed time. For a given time, the radius value associated with each data point represents that of the bisecting radius of each capacitor.

The middle row of graphs plot the concentration calculated for each capacitor versus time. C1 is associated with the outermost annulus. As such, its concentration is the fastest to rise during soaking and likewise to fall during bakeout.

The bottom row of graphs plots the total mass of absorbed moisture vs time. It is calculated using Eqn. 3, below.

$$(3)\quad M_{H_2O} = \sum_{i=1}^{4} Conc_i \bullet C_i$$

(Note that the equivalent equation in Part 1 (Eqn. 4) had a prefactor equal to 2 to compensate for the half symmetry of the 1-D model.)

The results for the soak process in Case 1 are worth noting. In spite of the 500 hr duration, the moisture concentration at the center of the sample reached only about half of its saturation value. This is simply due to the rather large radius on the modeled sample, equal to 0.56 mm. By comparison, in Part 1, the diffusion length between the mid-plane and the exterior surface of the sample was 0.012 mm. Here, full saturation was achieved in only about 4 hours.

The bakeout process for these two cases assumes the use of an oven set to a temperature of 105˚C. Since the oven is assumed to be open to the atmosphere, in the vicinity of the BT, a very low RH value of 0.4% is calculated. At this high temperature, the diffusion coefficient is high enough that the bakeout is complete at approximately 650 hrs. This was nearly independent of the initial moisture content of the BT at the start of bakeout.

The bakeout process for Cases 3-6 are more representative of conditions in application environments. In all four cases, the temperature of the BT was assumed to be 60˚C, which was higher than the ambient temperature in each case.

Cases 3 and 4 assume an ambient temperature of 20˚C, at RH values of 20% and 40%, respectively. These would be considered rather mild application environments and would be representative of ASHRAE data center guidelines of today. These results are displayed in Figure 5. The time required for the moisture content to reach a steady minimum is nearly 5000 hours. As mentioned, this is probably a conservative estimate. However, it is indicative of a much slower drying process than in a dedicated bakeout oven. One notes, also, the beginning of a trend in that the residual moisture level in the BT is greater than the near zero value obtained in the bakeout oven. These

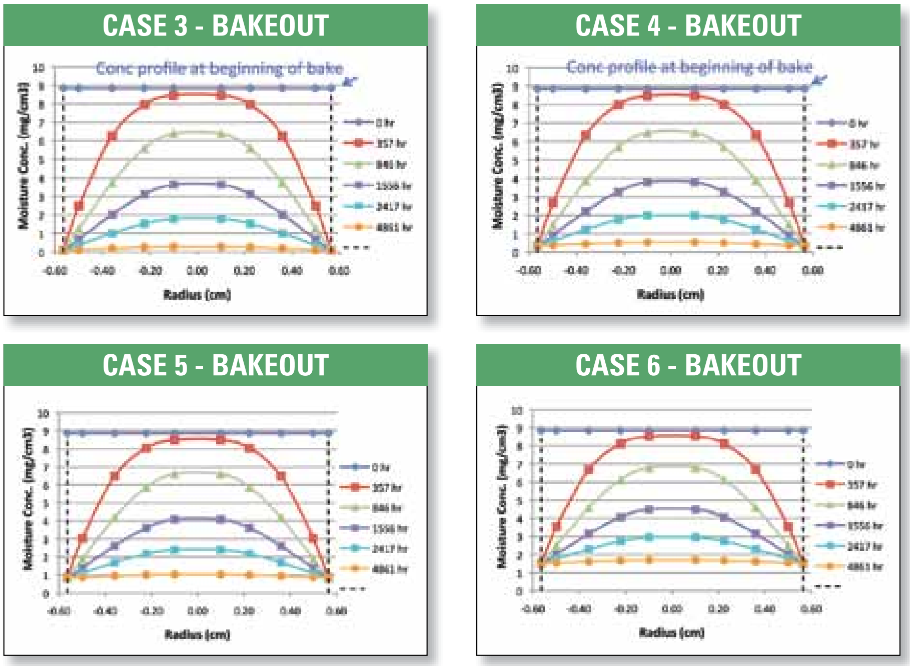

FIGURE 5: Solution results for BT samples, Cases 3 - 6, showing change in diffusion profile versus time due to bakeout process at varying ambient temperature and RH values

TABLE 3: ENVIRONMENTAL CONDITIONS ASSUMED IN DIFFUSION CASE STUDIES

<table>
<tr><th rowspan="3">Case #</th><th colspan="3">SOAK CONDITIONS</th><th colspan="5">BAKEOUT CONDITIONS</th></tr>
<tr><th>Temperature/ Relative Humidity</th><th>Soak Time</th><th>Conc @ BT/Air Interface</th><th>Air Temp</th><th>Air RH</th><th>BT Temp</th><th>RH @ BT/Air Interface</th><th>Conc @ BT / Air Interface</th></tr>
<tr><th>(°C/% RH)</th><th>(hrs)</th><th>(mg/cm^3)</th><th>(°C)</th><th>(%)</th><th>(°C)</th><th>(%)</th><th>(mg/cm^3)</th></tr>
<tr><td>1</td><td>85/85</td><td>500</td><td>8.85</td><td>20</td><td>20%</td><td>105</td><td>0.4%</td><td>0.00</td></tr>
<tr><td>2</td><td rowspan="5">85/85</td><td rowspan="5">To Satur-ation</td><td rowspan="5">8.85</td><td>20</td><td>20%</td><td>105</td><td>0.4%</td><td>0.00</td></tr>
<tr><td>3</td><td>20</td><td>20%</td><td>60</td><td>2.4%</td><td>0.07</td></tr>
<tr><td>4</td><td>20</td><td>60%</td><td>60</td><td>7.1%</td><td>0.33</td></tr>
<tr><td>5</td><td>40</td><td>40%</td><td>60</td><td>14.8%</td><td>0.83</td></tr>
<tr><td>6</td><td>40</td><td>60%</td><td>60</td><td>22.2%</td><td>1.52</td></tr>
</table>

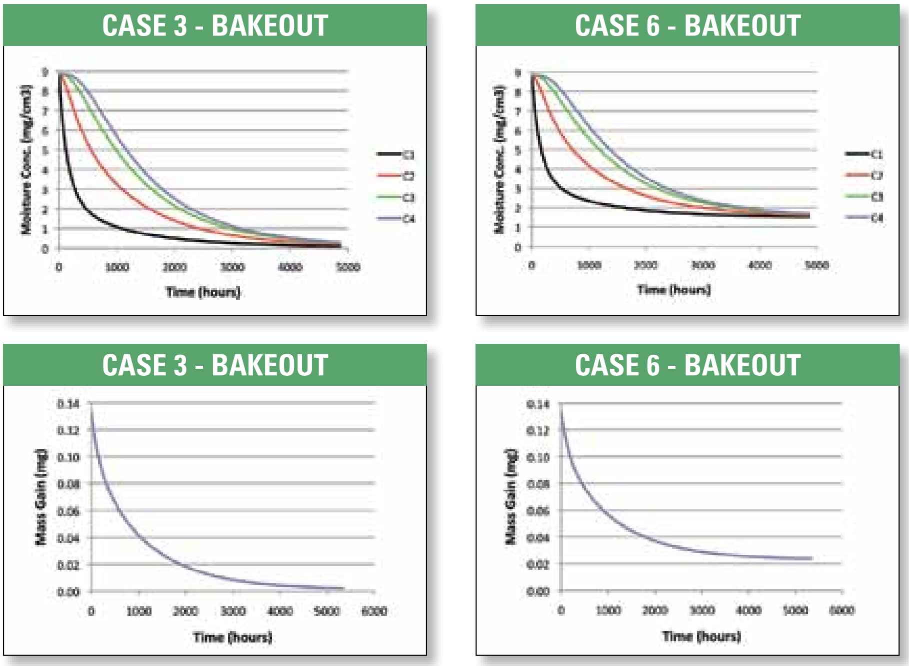

FIGURE 6: Additional plots of Cases 3 and 6: moisture concentration values at each capacitor versus time and mass gain curve versus time. These Cases represent the two extremes of those in Figure 5: Case 3, minimum residual moisture; Case 6, maximum residual moisture."

residual moisture concentration levels were calculated at 0.07 and 0.3 mg/cm^3, respectively.

There is a trend among data centers to push ambient temperature and RH values to higher levels in the interest of improving data center cooling efficiency. ASHRAE has been supportive of this trend by relaxing temperature and humidity guidelines and allowing temperatures in the 40 to 45˚C range, with appropriate controls on humidity [5]. Cases 5 and 6 assume an ambient temperature of 40˚C and RH levels of 40 and 60%, respectively. The results in Figure 5 indicate a similar time for the residual moisture to reach a stable value. This should not be a surprise, since this is largely the result of the BT temperature, since this determines the diffusion coefficient. However, the residual concentration values of 0.8 and 1.5 mg/cm^3 are significantly higher than those associated with the 20˚C ambient.

CONCLUSIONS

Computationally efficient methods have been demonstrated that are useful in calculating moisture diffusion rates for simple geometries over a wide range of ambient conditions of temperature and humidity.

The use of ambient air with elevated temperature and humidity levels for cooling electronic components containing organic materials has been shown to promote a higher concentration of residual moisture in these materials. It behooves the industry to not only quantify moisture levels in organic materials more effectively, but also to better understand the impact of increased moisture levels on the reliability and electrical performance of these materials.

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Featured

Measuring and Predicting Junction Temperature:
Thermal Factors Influencing Reliability in GaN HEMTs

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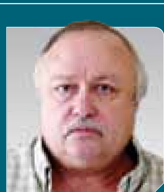
Andrew Trageser has more than 32 years of experience in product development and new product manufacturing, including 22 years in engineering management and business leadership. With aluminum company Alcoa, Trageser was involved with the design, manufacture, and recycling of a wide variety of aluminum products. He is the recipient of 12 patents in the areas of manufacturing processes and product design, and led a $30 million corporate profitability reporting initiative using activity-based costing. After joining Penn State EOC in 2009, he was named the technical director of the EO ManTech Center of Excellence, turning his creative attention to reducing costs in the manufacture of Navy systems.



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1. INTRODUCTION

AS A NASCENT technology compared to GaAs, Si, or nonsolid state technology, GaN-on-SiC transistors have not established a history of reliability from which end-users of the technology can establish its long term replacement and refurbishment costs [1]. Nonetheless, GaN provides a number of distinct advantages over older technologies, including improved heat transfer properties, wider bandgap energy, higher operational temperatures, and higher frequency performance [2].

In lieu of historical reliability information, the consumers of this technology must depend on accelerated lifetime testing (ALT) of parts where a predicted operational lifetime, on the order of millions of hours, is extrapolated from faster failures (hundreds of hours) achieved at highly elevated temperatures. The validity of this extrapolation is dependent on three assumptions: 1) that the physics of failure for the GaN device is analogous to previous technologies (i.e., defect diffusion driven by thermal gradients), allowing for a loglinear extrapolation (the Arrhenius model) through time-temperature space, 2) that the ALT is exciting the same predominant failure as occurs in fielded devices under standard operating conditions, and 3) that the operational temperature of the device is known [3].

This paper focuses on this third assumption, using empirical (micro-Raman thermography, transient thermal Testing [4], and midwave infrared thermography) and finite-difference modeling [5] techniques to assess the measure, spatial uniformity, and statistical variability in temperature measurements on GaN transistor devices. For our purposes, we are accepting the first two assumptions are true and focusing on the impact of thermal variability and the underlying uncertainty it creates in a thermally-diffused failure model

2. THE ARRHENIUS RELIABILITY MODEL

The activation of thermally-induced diffusive failures has been generally accepted by device manufacturers to follow an Arrhenius model whereby the time-to-failure and device operating junction temperature are related by the relationship:

(1) $t_{failure} = Ae^{\frac{Ea}{RT}}$

where $t_{failure}$ is the time-to-failure, E_a is the failure activation energy, R is the Boltzmann constant, and T_j is the device junction temperature. If the log of both sides of (1) is taken, then the following lognormal relationship is determined:

(2) $\log t_{failure} = \log A + BT^{-1}$
where $B = E_a / R$.

In practice, the operational lifetime of a device is predicted by stressing the device at elevated temperatures well beyond the typical operating temperature. At these elevated temperatures, the device fails faster than it would at operational conditions allowing researchers to complete the tests in time spans of tens to thousands of hours as opposed to the millions to tens of millions of hours one expects the device to last under fielded operating conditions. The rate of those failures is used to determine the values for A and B, which are the y-intercept and slope of equation (2), respectively.

However, the accuracy of the Arrhenius model is dependent on the certainty with which one ascertains the device junction temperature, among other factors. The extrapolation of the Arrhenius model along a lognormal plot across several decades of time is highly sensitive to the placement of the temperature-failure time data under the accelerated life testing (Figure 1). As shown in this paper, the inability to sample a device set and measure device temperature to a high degree of confidence can lead to a large uncertainty as to the predicted lifetime of the device.

3. EXPERIMENTAL DESCRIPTION

Two hundred discrete GaN-on-SiC high electron mobility transistors (HEMTs) were purchased from a commercial source and then packaged by a separate commercial entity. Twenty of those packaged devices were sampled from the population and run through a battery of three empirical tests: 1) mid-wave infrared (IR) thermography, 2) transient thermal testing (TTT), and 3) micro-Raman thermography (μRT).

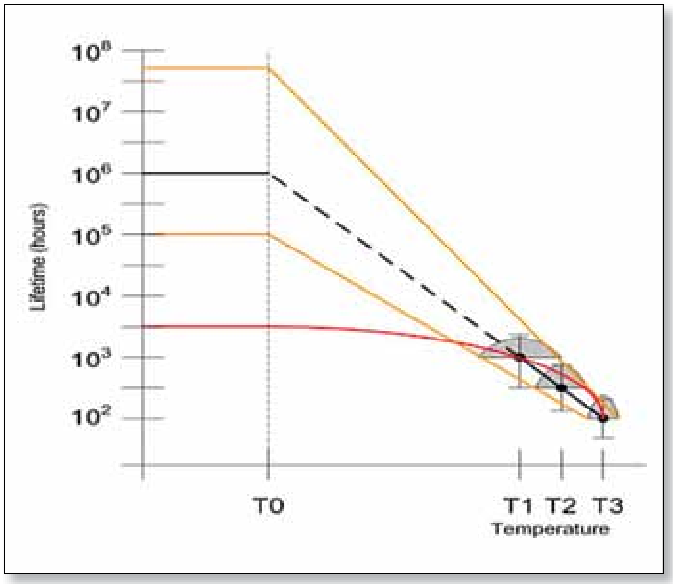

FIGURE 1: Arrhenius operational life prediction (@ T0) using data extrapolated from accelerated life test data (black). Orange curves show effect of uncertainty in device junction temperature on predicted lifetime. The red curve shows a potential outcome of a set of devices where the log-linear extrapolation assumption is not valid.

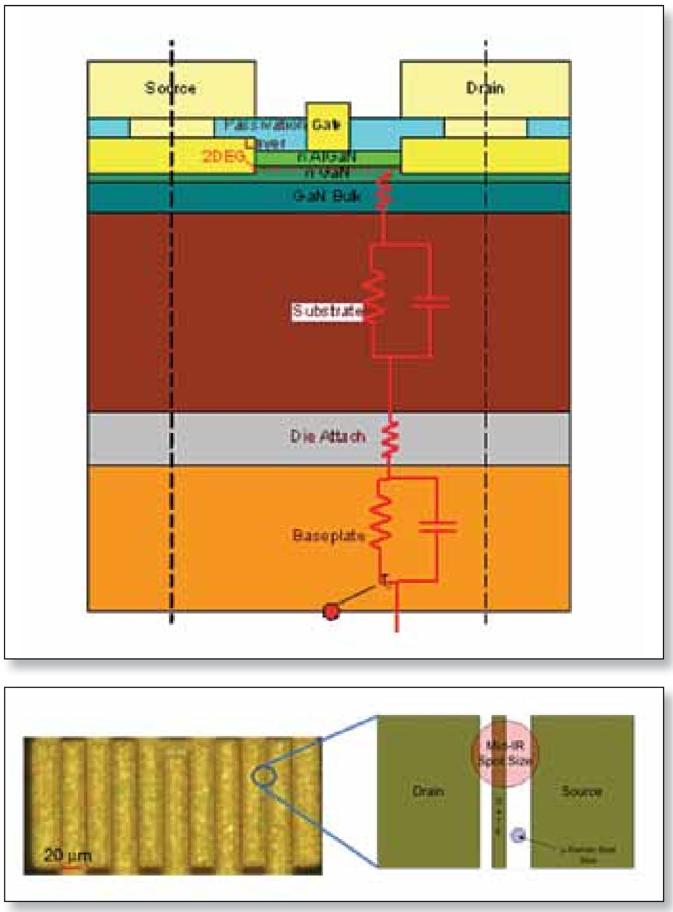

FIGURE 2:(Top) Schematic of the device cross section including heat flow path and (bottom) top view of device with schematic magnification of a finger with corresponding measurement technique spatial resolutions.

The average thermal resistance is given by the following equation

$$(3)\quad Rt=\frac{T_{meas}-T_{coolant}}{P_{diss}}$$

where T_{meas} is the measured temperature, $T_{coolant}$ is the ambient coolant temperature of the heat sink, and Pdiss is the power dissipated across the device (drain current times drain voltage). It is recognized that some uncertainty in the measurement of $T_{coolant}$ and P_{diss} exists but that this uncertainty is negligible compared to the uncertainty in T_{meas}.

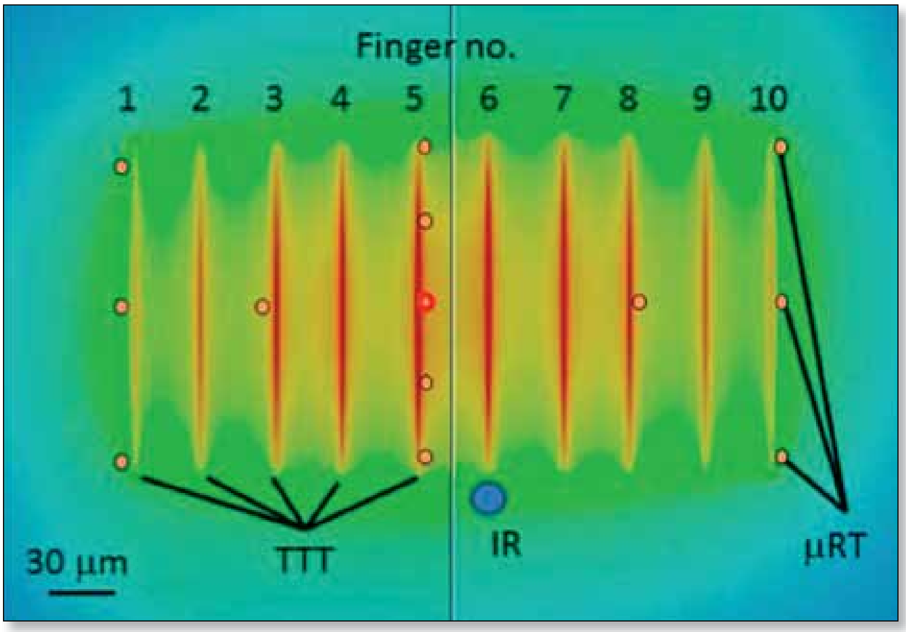

FIGURE 3: Location of empirical measurements for each technique – Infrared (IR), micro-Raman thermography (µRT), and transient thermal tester (TTT) on computationally simulated temperature contour plot of device junction plane.

Since each of the empirical techniques measures temperature at different locations on the device surface (Figure 3), the expectation is that each method will capture different temperatures.

The IR measurement, which was obtained using a mid wave (3-5µm) sensor, provided a minimum spatial resolution of about 10µm, larger than the distance between the gap between the gate metallization and the drain (Figure 2). Thus this measurement was made farthest from the device gate where most of the heat is generated, and so should result in the lowest temperatures. Conversely, the µRT measurement, performed with a 488nm laser, provides spatial resolution on the order of 750 nm. Thus this technique can resolve the gap between the gate and drain metallization and should come closest to capturing the peak device junction temperature. The third technique, the transient thermal tester, is a non-optical technique which measured the electrical response of a device to an electrical excitation in order to deduce the thermal resistance-capacitance network that must exist. This technique measures the average response across the entire active region of the device, and so, the TTT and spatially averaged µRT measurements should compare closely, as both sample across the gates and provide device junction temperature from both colder and warmer regions of the device.

A fully three-dimensional computational fluid dynamics model was also performed (Figure 3) using property and geometric data from the device manufacturer, packaging manu-

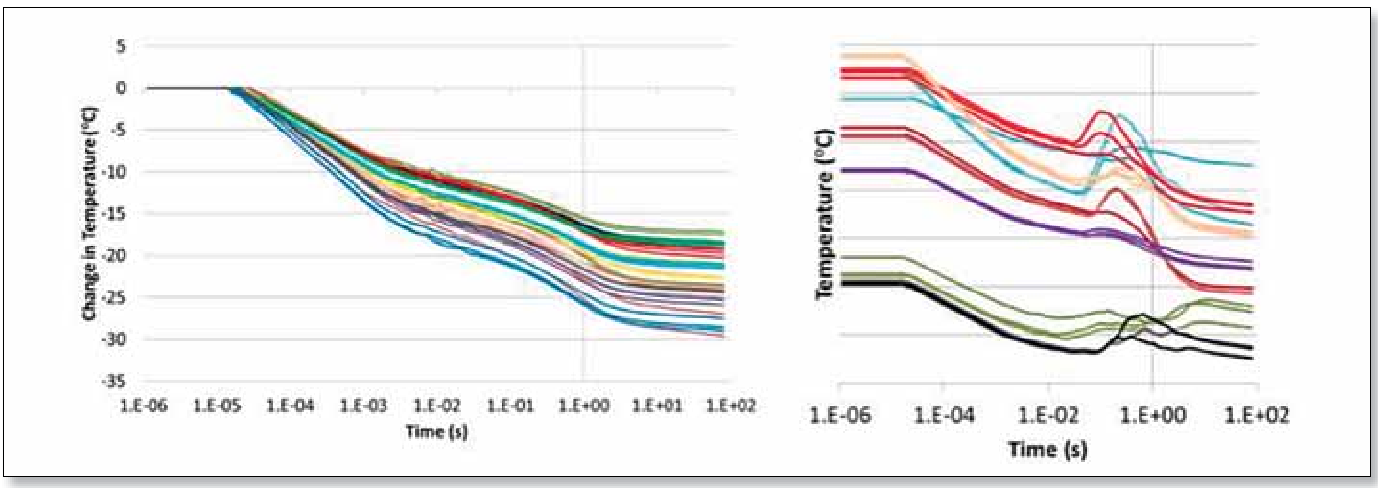

FIGURE 4: Thermo-electrical response of devices to the electrical step using the TTT approach. Note that subset of tested devices on the right shows a non-thermal electrical response between 10 ms and 1s.

Finger No:	1	3	5	8	10
Source End	10.45		13.55		10.12
1/4			13.17		
Center	11.75	12.65	13.01	12.75	11.08
3/4			12.47		
Drain End	9.51		10.26		8.69

TABLE 1: Thermal resistance (K/W) for each prescribed micro-Raman measurement location and averaged across 19 devices. Finger location as indicated in Figure 2.

facturer and from open literature sources.

All geometric detail was included in the model around the device periphery. The heat generation site was modeled as a small volume directly under the gate metallization along the plane of the two-dimensional electron gas (2DEG) and the baseplate of the device was modeled with an isothermal boundary condition.

4. RESULTS

Since the devices are experiencing a step down in drain current, the device temperature should decrease steadily from a hot state to a cool state, corresponding to a steady decline in voltage. For a majority (13 of 20) of the devices, this steady decline was evidenced as seen in Figure 3. Each tested device corresponds to a color and each trace of a particular color represents one of the three tests for that device. Note that the colors are tightly spaced, which indicates good experimental repeatability. The spread of the thermal transient curves after 100 seconds is about 13°C across the 13 tested devices. This corresponds to a range in thermal resistance across the sample of 9-13 K/W.

However, a subsample of the devices exhibited a nonthermal phenomenon at a time on the order of 10 ms to 1 s after the step down, where the drain voltage increased (Figure 4, right). Since there is no source of additional heating that could cause the voltage to increase, the phenomenon must be a non-thermal electrical phenomenon. At the point of this writing, the cause of that phenomenon is not clear. One unverified suspicion is that charge trapping in the device is a potential culprit.

Micro-Raman results were studied in two ways, 1) attaining the peak point temperature measured of the 13 prescribed locations and 2) a spatially-averaged measure across the 13 measured points. The peak temperature should be indicative of the hottest temperature on the active device, which in theory, is thought to drive device failure. Based on an idealized model, the expectation is that the peak temperature should be the center-most location on the centermost gate finger. In practice, the Raman measurements do not necessarily follow that pattern. Across this sample of 19 devices (one device proved impossible to measure due to topological variability scattering the Raman signal), the peak temperature for the device occurred at 7 of the 13 prescribed points. Most of the peak temperature measurements were made along the center gate finger (12 of 19) and only 1 occurred along the perimeter finger. If the temperature at each of the 13 locations is averaged across the 19 devices, the thermal resistance measurement for each point appears in Table 1.

When averaged across the device sample set, the predicted thermal gradient perpendicular to the gate fingers is seen em-

	Mean Rt	St. Dev	Tj-Tb range @ 68% confidence
	(K/W)	(K/W)	(K)
IR	8.5	1.5	28 < T < 40
TTT	11.4	1.1	41 < T < 50
µRT avg	11.5	2.4	36 < T < 56
µRT peak	15.0	2.9	48 < T < 72
CFD Model	15.3		

TABLE 2: Summary of statistics for device thermal resistance as a function of measurement technique.

pirically. However, the predicted parallel gradient is not seen along the center finger. Along that finger, the hottest location does not appear to be at the finger center, but at the source end of the finger. This deviation from prediction may be due to the model simplification where metallization off the ends of the gate fingers were not included.

The Raman measurements have the highest standard deviation of the three empirical techniques, due to several factors: 1) the high precision of the technique combined with a limited sampling of spatial data points on the device surface (as compared to the TTT technique which is an analog measurement across the entire device) and 2) a high sensitivity to topological variability across the device surface. Nonetheless, the peak Raman measurement assesses a thermal resistance within 5% of the device manufacturer's specified thermal resistance for this family of devices. Furthermore, it is worth noting how closely the average Raman measured thermal resistance (11.5 K/W) compares to the TTT approach (11.4 K/W), confirming expectations (Table 2).

The initial CFD model underpredicted the device vendor specified thermal resistance within 5%. Relating this information back to Figure 1, an unfortunate selection of devices could result in a significant portion of a radar system failing an order of magnitude or more sooner than expected based on the mean-time-to-failure data generally supplied by the manufacturer.

5. CONCLUSIONS

A multi-tool approach to assessing device junction temperature and thermal performance has been shown. Each tool provides different information and uncertainties so that such a broad empirical assessment is important to determine junction temperature and thermal performance. The thermal variability of packaged devices can be high. As such, an end user must view the assumption that the device junction temperature is known in the assessment of the Arrhenius reliability model with a degree of skepticism (Table 2).

To increase confidence in accounting for such uncertainty one should consider:

- Instituting part-specific thermal models
- Increasing statistical sampling – use additional acquisition cost to defray future refurbishment cost
- Monitoring quality improvements in manufacturing and packaging processes

ACKNOWLEDGMENTS

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Benefits and Drawbacks of Using Two-Phase Cooling Technologies in Military platforms

Johannes van Es, Henk Jan van Gerner, National Aerospace Laboratory NLR, Netherlands

THE NEXT GENERATION military platforms will be equipped with more and more powerful sensors and avionics. The increasing power densities in electronic subsystems demand more cooling power while survivability requirements limit the possibilities for extending or adding cooling systems. This trend inevitably leads to thermal challenges which need to be solved. There are two main approaches for solving these problems. The first aims to increase the cooling capacity of the system. It is most practical for new platforms. The second approach, more suitable for upgrades of existing platforms, is to optimize the systems to enable them to fully exploit their existing capabilities. One of the focal points will be the reduction of the temperature drop between the dissipating electronics and the heat sink as illustrated in Figure 1.

In this article, an overview of the different types of two-phase cooling systems is given, including the main advantages and drawbacks, and examples of their use.

HEAT PIPES

The most well-known two-phase heat transport system is the heat pipe [2]. A heat pipe is a closed pipe filled with vapor and liquid of a dedicated working fluid. On the walls of the heat pipe a capillary structure is implemented (axial grooves and/or a capillary wick) and therefore contains the liquid in the pipe.

On one end of the heat pipe dissipating electronics are attached. The dissipated heat evaporates the liquid, and absorbs the heat. By the creation of the additional vapor the vapor flows to the other side of the heat pipe where it condenses and subsequently rejects the heat. The liquid is pumped back by capillary action closing the loop. Because the evaporation and condensation "occurs" at the same temperature the temperature drop over the pipe is only a few degrees induced by the vapor pressure drop over the pipe. Heat pipes are widely used in terrestrial design (laptops, CPU-cooling) and spacecraft thermal design (heat pipe radiators). The main drawback of heat pipes is their poor performance when used against gravity.

THERMOSYPHONS

A special type of heat pipe is the thermosyphon. A thermosyphon is a heat pipe which uses gravity to transport the liquid. The heat is therefore always collected and evaporated on the bottom side and condensed at the top side where the heat is removed by forced cooling or radiation. The liquid flows back to the bottom to close the loop. Thermosyphons are for example used in mountainous areas to keep roads or railways snow-free. The design is straightforward and robust, however even more dependent on orientation than a normal heat pipe.

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Henk Jan van Gerner is a research engineer at the Thermal Control Group of the NLR. He has extensive experience in the design and development of advanced two-phase cooling systems for both terrestrial and space applications. His current work is focused on the development of lightweight vapour-compression cycles, numerical modeling of pumped two-phase cooling systems, and systems with very accurate temperature control (0.001°C accuracy) at varying heat loads. van Gerner studied mechanical engineering and obtained his Ph.D. in the Physics of Fluids group at Twente University in the Netherlands.

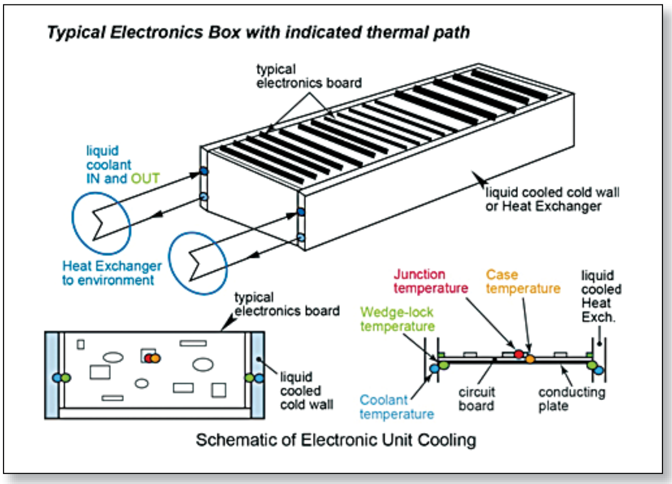

FIGURE 1a: Typical electronics box with indicated thermal path from junction to ambient air.
Red: junction temperature, orange: case temperature, green: wedge-lock temperature, light blue: coolant temperature after collecting the heat from the electronics, dark blue: coolant temperature cold side, purple: environment temperature.
Remark: A wedge-lock is rugged fastener or card retainer used to clamp a PCB within electronics box slot [1].

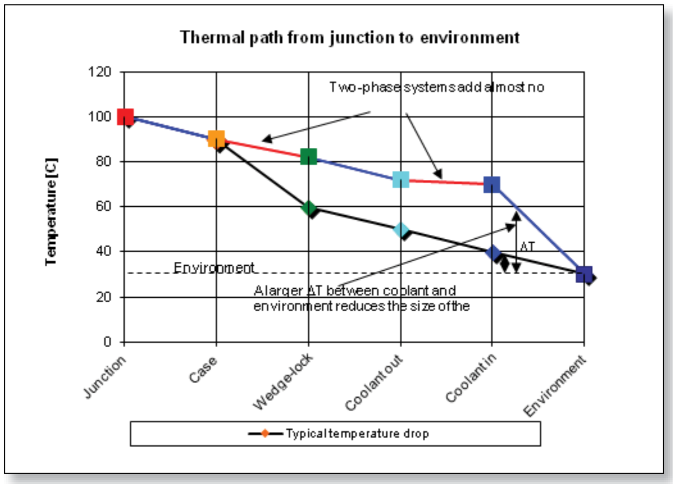

FIGURE 1b: Typical temperature drop from junction to environment. The lower line shows a system without two-phase technology implemented. The upper line shows a system with two two-phase systems implemented indicated with red line segments. A heat pipe system is integrated in the electronics board between case and wedge-lock and a two-phase pumped system is integrated to replace a liquid cooling system. This results in a lower ΔT. A reduced temperature drop allows to reject/transfer the dissipated heat at a higher temperature level to the environment. This can relax the overall cooling system requirements.

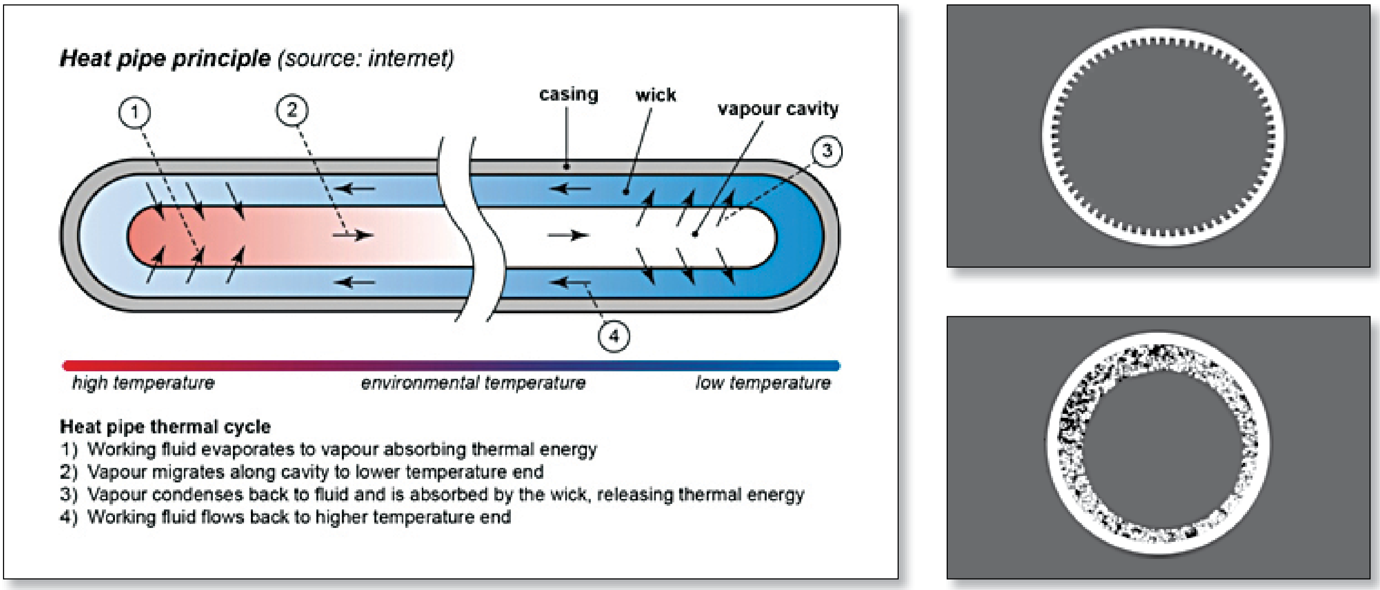

FIGURE 2 (a) Heat pipe working principle (Source: Wikipedia), **(b,c)** typical cross sections of commercially available heat pipes.

VAPOR CHAMBERS

A less common type of heat pipe is the vapor chamber. In fact it is a flat heat pipe with a very small length over diameter ratio. Vapor chambers are used to increase heat transfer of heat sinks, for example to enhance CPU- or power electronics cooling. Vapor chambers are gravity dependent but flat versions or types with the right wick design can be ruggedized to withstand acceleration forces. This type of heat pipes are mainly used as heat spreader but can also be used for accurate (mK-level) temperature control.

LOOP HEAT PIPES (LHP) AND CAPILLARY PUMPED LOOPS (CPL)

The Loop Heat Pipe (LHP) and Capillary Pumped Loop (CPL) are more advanced types of heat pipes. These loops separate, concentrate and optimize the capillary pumping action in the evaporator section (See Figure 3).

LHP's and CPL's can therefore provide more pumping power and work to a certain extent (few meters) against gravity. Main difference between the LHP and CPL is that the CPL has a separate temperature controlled reservoir which can dictate the saturation temperature in the evaporator and therefore set the payload temperature. In a LHP the reservoir (or compensation chamber) and evaporator are combined, this gives an advantage in starting up over the CPL as the wick of the evaporator is wetted in all conditions. Drawback of the LHP is the variation in payload temperature with payload power. LHP's are available over a large range of heat transport capacities (10W to 1kW), and are used extensively in satellite design and ground-based applications and also in specific applications for fighter aircraft (F-16 and UAV's).

Another drawback of LHP's and CPL's is the difficulty to extend them to multi-evaporator systems. Extensive research to multi-evaporator LHP's has been performed [4]

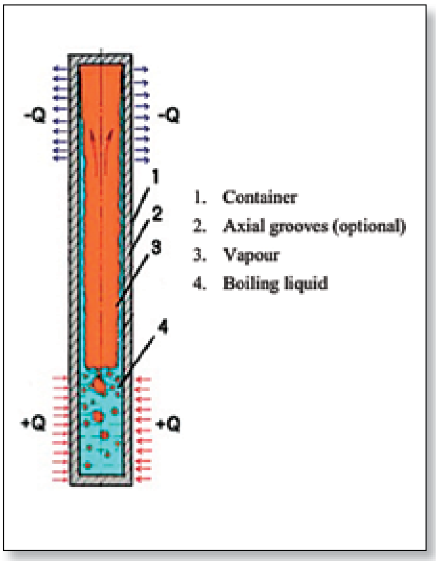

FIGURE 2.1: Thermosyphon principle (Courtesy: Kiev Research and technology centre).

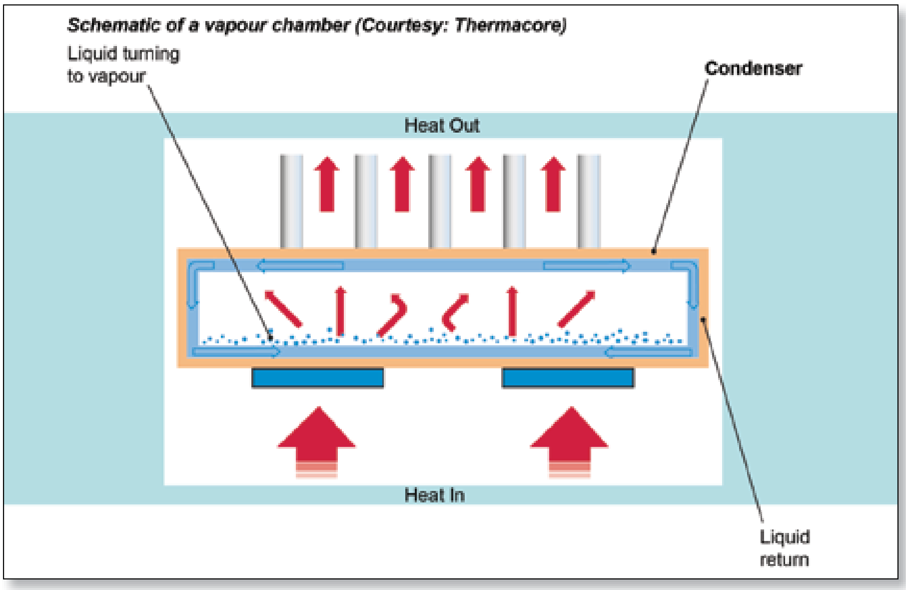

FIGURE 2.2: Schematic of a vapour chamber (Courtesy: Thermacore).

which resulted in improved designs but it did not lead yet to implementations.

TWO-PHASE MECHANICALLY PUMPED LOOP (2Φ-MPL)

Instead of capillary pumping forces also a mechanical pump can be implemented in a two-phase loop. The schematic is shown in Figure 4. Main components are an accumulator, an evaporator and a condenser section, a heat exchanger (optional) and of course a pump. The accumulator is temperature- or pressure controlled and sets the evaporation temperature. Although the pump adds complexity and a lifetime issue this system has considerable advantages.

The system is very flexible, the heat sources and heat sink can be located anywhere in the system and the heat load can be transported over large distances. Furthermore, the temperature of the heat sources can be accurately controlled. Because of these advantages, a two-phase mechanically pumped loop was selected as the only feasible concept for the Tracker Thermal Control System (TTCS) of the AMS02 experiment [5], a development lead by NLR [6]. This system was launched with the space shuttle (STS-134, May 2011) and subsequently mounted on the International Space Station for a 15 year mission. The system provides <0.2˚C temperature stability for the payload in an environment with large temperature variations. Recent terrestrial test-setups even achieve <0.001˚C temperature stability with changing heat loads. 2Φ-MPL can be used to transport small (10 W) to very large (MW) heat loads. In view of the pump electronics mass 2Φ-MPL's are most suitable for navy and land-based applications requiring accurate temperature control (e.g. active antennas). When smaller pumps with more compact electronics are developed 2Φ-MPL's will also become attractive for air-based and satellite platforms.

OSCILLATING HEAT PIPES (OHP)

A special two-phase system is the Oscillating Heat Pipe (OHP) [7-11].

Despite its name the OHP-principle is completely different from a heat pipe. An Oscillating Heat Pipe is a meandering tube with a diameter between 0.25 and 2 mm. As a result of capillary forces, the tube is filled with liquid and vapor plugs of a working fluid (see Figure 5). Heat is transported in the OHP by the oscillation of the plugs in the OHP. This oscillatory motion is driven by the generation and the expansion of vapor bubbles and the inertia of the plugs. Heat is transported from the hot to the cold side mainly by the sensible heat of the liquid, and the temperature drop along an OHP is approximately 10-15°C. This is a much larger temperature drop than for a classical heat pipe. An interesting feature of the OHP is that it can operate under high g-loads [10]. The NLR developed Flat Swinging Heat Pipe (FSHP) has been tested upto 8.4g without decrease in performance. Until now OHP's are only implemented on a small scale e.g. for CPU cooling [12].

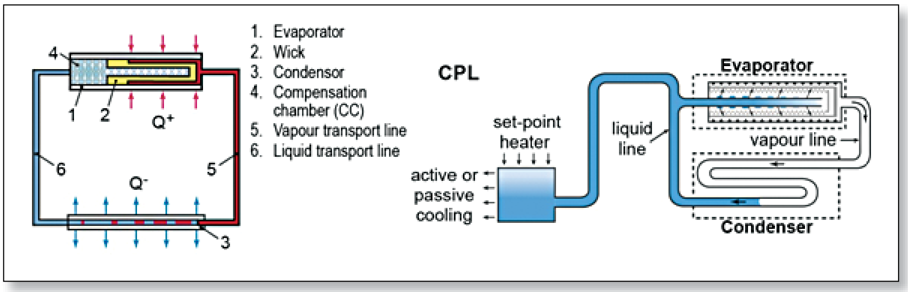

FIGURE 3: LHP [3] (left) and CPL (right) principle (Courtesy: Swales).

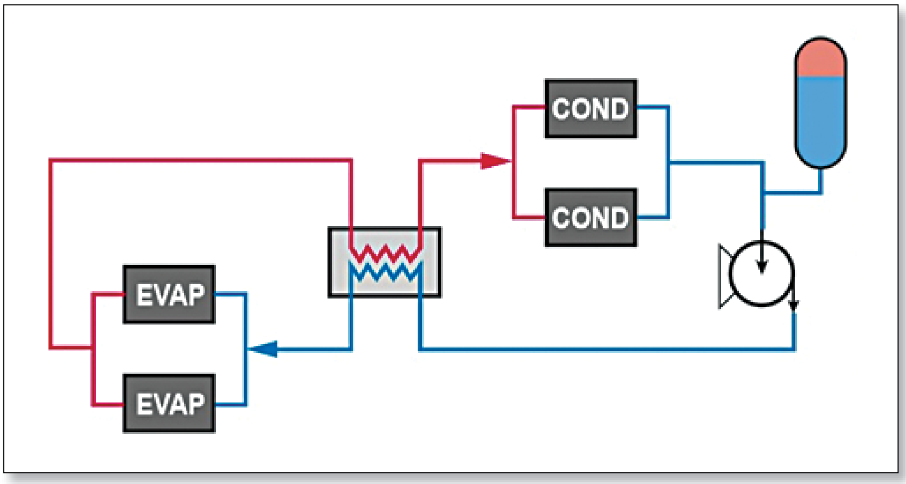

FIGURE 4: Schematic drawing of a 2Φ-MPL with parallel evaporators and condensers. (Parallel evaporators can cause flow instabilities with large difference in heat loads. In the TTCS system the heat loads were similar).

ADVANTAGES AND DRAWBACKS OF TWO-PHASE HEAT TRANSPORT SYSTEMS

To elucidate where the above listed two-phase systems are best suited, first the disadvantages are discussed. Main general disadvantages of two-phase systems for use in military platforms are:

- Gravity dependence
- Inflexibility of the interface to the payload (evaporator)

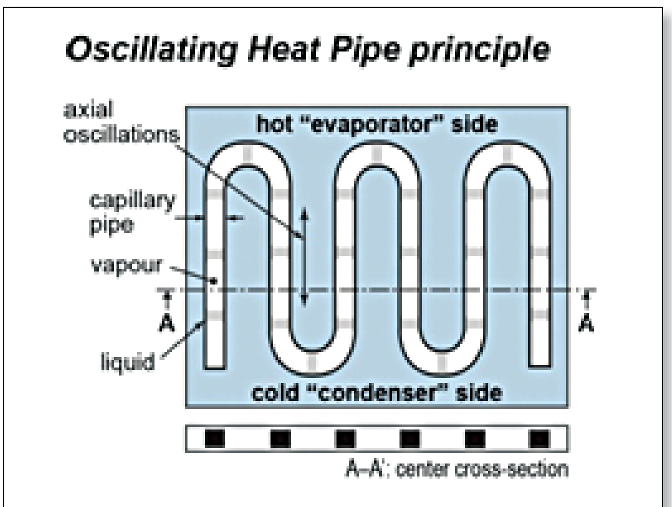

FIGURE 5: Schematic drawing of an OHP.

The gravity dependence makes the use of general heat pipes and thermosyphons only possible in gravity assisted and zero-gravity environments and therefore unsuitable for air-based platforms. Some special heat pipe designs are available but the transport length is limited or in case of OHP's the performance is much lower. LHP's and CPL's can withstand high-g forces and are therefore also suitable for aircraft applications. The inflexibility of payload interface is the second general drawback of two-phase heat transport systems. Evaporation sections of heat pipes themselves are flexible enough and are therefore implemented in an extensive amount of satellite, marine and ground-based designs. The concentrated LHP and CPL evaporator sections are however bulky and limited in length. Therefore sensors or other payloads with distributed elements are not easy to cover by one or two LHP evaporators. In satellite applications combined HP-LHP networks are successfully used to cope with this problem at the cost of extensive test campaigns. In aircraft design heat pipe networks are not feasible in view of the gravity problems, therefore only single LHP evaporators are used for concentrated payload sensors. For payload sensors with more distributed electronics the 2Φ-MPL's are a feasible option as the evaporator can facilitate multiple widespread sensors with only small diameter (1-8 mm) tubing. The 2Φ-MPL's bulky accumulator and pump section can be located far away from

Two-phase system platform design guideline

	Land and Marine-based	Airborne platforms	Spacecraft
Heat pipes	gravity assisted only	limited length	excellent
Thermosyphons	gravity assisted only	not possible	not possible
LHP's and CPL's	specific benefits are not used	good	excellent
OHP's	relative low performance	good in confined locations	in specific cases
2Φ-MPL's	accurate T-control	accurate T-control	accurate T-control
Vapour chambers	as heat spreader	as heat spreader	as heat spreader

= excellent = in specific conditions = not preferred = not possible

Two-phase system payload design guideline

	Centralised pay-load	Distributed pay-load	Pay-load with confined access
Heat pipes	limited heat flux	in case of enough access	not preferred
Thermosyphons	good	not preferred	not preferred
LHP's and CPL's	good	not preferred	not possible
OHP's	not preferred	not preferred	good but limited in length
2Φ-MPL's	not preferred	excellent but adds mass	excellent
Vapour chambers	as heat spreader	not preferred	not possible

= excellent = in specific conditions = not preferred = not possible

the payload. This makes 2Φ-MPL specifically suitable for implementation in existing payloads for platform upgrades.

Two-phase systems would not be so popular if there were no clear benefits. The most well-known advantage is the mass effectiveness. As the latent heat of most fluids is at least one or two orders larger than the sensible heat, a two-phase heat transport system can transport considerably more heat per fluid mass resulting in a lower system mass and smaller cooling tubes. This led to the extensive application of heat pipes and loop heat pipes in spacecraft and aircraft design as in these platforms mass is a driving requirement.

The second clear but less well-known advantage is the high temperature stability of two-phase heat transport systems. As two-phase systems make use of evaporation (boiling) of a liquid and boiling always happens at one temperature, two-phase systems can perfectly control delicate payloads on a stable temperature (e.g. active antennas and radar applications).

ROUGH TWO-PHASE DESIGN GUIDELINE

In the two tables above, rough guidelines for system engineers are given to identify which type of two-phase heat transport system would fit best for their type of platform and payload. In the tables above, the applicability of the types of two-phase systems for the different platforms is summarized. The main selection driver in the first table is the gravity dependence.

In the second table a rough division in payloads is made based on their lay-out of heat sources. A centralised payload is a payload with a concentrated heat source like a linear motor. A distributed payload has a large number of widespread heat sources like active antennas or SAR radar applications. Finally a third type of payload is defined with confined access.

CONCLUSIONS

An overview is given of two-phase heat transport systems with benefits and drawbacks of the systems. Rough design guidelines are given for the applicability of the several systems for airborne, land-based and navy platforms. By checking the application in the two tables a system engineer can judge whether a two-phase system is available and he can already make a pre-selection.

Although two-phase systems are already used in many military platforms, there are still improvements needed to increase the application range. To advance the introduction of 2Φ-MPL's in platforms and platform upgrades, it is needed to reduce the pump (electronics) mass and increase the pump reliability.

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Measured Thermal Resistance of Microbumps in 3D Chip Stacks

Evan Colgan, Jamil Wakil, IBM

INTRODUCTION

AS IT BECOMES increasingly difficult to scale devices down to improve performance, alternate approaches such as 3D chip stacks are being developed, which improve system performance by increasing the interconnect density and reducing the interconnect length(1). The stacking of multiple chips with through silicon vias (TSV) and fine pitch microbumps between them not only increases the bandwidth and reduces the latency between the chips, but it also increases the difficulty of adequately cooling the devices during operation.

With a conventional lid-less chip package, Fig. 1(a), the thermal path from the active circuits is through the silicon substrate, which can act as a heat spreader, and through the thermal interface material (TIM) layer to the heat sink. Typically, only a small fraction of the heat flows through the back-end-of-line (BEOL) wiring layers on the chip and the solder bumps into the package substrate. With a 3D chip stack, the heat from multiple chips is now being removed through the back surface of the top chip and both the BEOL wiring layers and the microbump layer between chips are in the thermal path, Fig. 1(b). Additionally, the chips that contain TSVs are thinned so that they are less effective at spreading heat from hot spots.

To be able to design systems based on 3D chip stacks, it is necessary to accurately characterize the additional thermal resistance from the BEOL and the microbump layers between chips. There have been extensive theoretical studies of the thermal resistance in 3D chip stacks (2-6), but only limited experimental measurements have been reported(7-9). In previous work(10), we reported on thermal resistance measurements in 4-layer chip stacks with ~25 μm diameter Pb-free solder microbumps with pitches of 50, 71, and 100 μm both with and without underfill.

THERMAL CHIP STACK DESIGN AND TESTING

The design of the thermal chip stack test vehicle is described in Fig. 2. The test vehicle consists of a ceramic substrate, a silicon carrier, and four thermal chips, shown schematically in Fig. 2(a). A cross-sectional image of an assembled thermal chip stack is shown in Fig. 2(b). The thermal chip, M1 heater, and M2 resistive temperature sensors dimensions are shown in Fig. 2(c). The thermal chips were joined together with ~ 25 μm diameter Pb-free solder microbumps, which had an average height of 16 μm after bonding. The underfill material used had a measured thermal conductivity of 0.55 W/m-K. The region above the heater was divided into nine 6 x 6 mm areas where the microbump pitch was 50 μm in the corner areas, 100 μm in the areas located along the center of each side, and 71 μm in the center area; see Fig. 2(c). The resistive temperature sensors were centered in each of these areas and were aligned above each other in the chip stack. As shown in Fig. 2(a),

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Jamil A. Wakil is currently working on data center thermal development for IBM systems, focusing on water cooling and energy efficiency. He joined the IBM Microelectronics packaging group in 1999, where he spent ten years on first level thermal development of organic packages and 3D stack packages. He holds an MS and Ph.D. in mechanical engineering from The University of Texas at Austin, a B.S. in mechanical engineering from Texas A&M University at College Station, and a B.S. in Electrical engineering from the University of Texas at Dallas. Jamil has eight patents and several refereed publications.

there were no TSVs through the thermal chips in the central area where the heater was located; the electrical connections between layers were all in the perimeter region. In addition to the silicon, a number of insulator layers were present on the top and bottom surfaces of the chips and in the thermal measurement region, see Fig. 3. The composition, thickness, and unit thermal resistance values are listed in Table 1. The unit thermal resistance through the chip is approximately 5.5 C-mm^2/W (10).

The thermal chip stack was characterized in a test station where the substrate was clamped to a hybrid LGA (land grid array) socket on a test card and a water cooled cold plate was coupled to the top of the chip stack by using a removable TIM material. The temperature of the water circulating through the cold plate was controlled by a recirculating chiller and monitored by the data acquisition system. Four-point resistance measurements were performed on all the resistive temperature sensors and a constant current source was used to power the heater. The sensor resistors were all individually calibrated by varying the water temperature, measuring the sensor resistor values, and performing a least-square-fit to the resulting data. The uncertainty in the measured thermal resistance is < 5% for the 50 μm pitch and < 10% for the 100 μm pitch regions and is mainly due to uncertainty in the sensor calibration and heat flowing into the substrate or spreading laterally rather than through the chip stack to the cold plate.

RESULTS & DISCUSSION

Results are shown in Fig. 4 for the chip stack, sample number G22, before underfill (a) and after underfill was applied (b). Power was supplied to the heater of the bottom chip of the stack (chip A, see Fig. 2a) and the temperate values were measured at the various temperature sensors in the chip stack. In Fig. 4(a,b), the sensor locations and microbump pitch are indicated on the x-axis, where NW, NE, etc refer to different areas of the chip. As would be expected, the chips lower down in the stack, i.e. further from the heat sink, are hotter. For the chip stack without underfill, the higher temperatures in area NE versus the other 50 micron pitch areas is believed to be due to variations in the thickness of the TIM layer between the chip stack and cold plate. Note that the temperature difference between adjacent chips increases as the pitch of the microbumps is increased. The temperature difference between chips is not directly comparable between the results without underfill and with underfill as the power applied was different.

The measured unit thermal resistance of ~25 μm diameter Pb-free microbumps with a pitch of 50 μm, 71 μm, and 100 μm both with and without underfill is plotted in Fig. 4(c). These results are from three thermal chip stacks, sample numbers G22, G24 & G25. For the 50 μm and 100 μm pitch areas, the results are only reported when three or four aligned sensor pairs are available across the specific microbump layer. For the 71 μm pitch area, only one sensor pair is available for each microbump layer. The unit thermal resistance values were calculated assuming no thermal spreading;

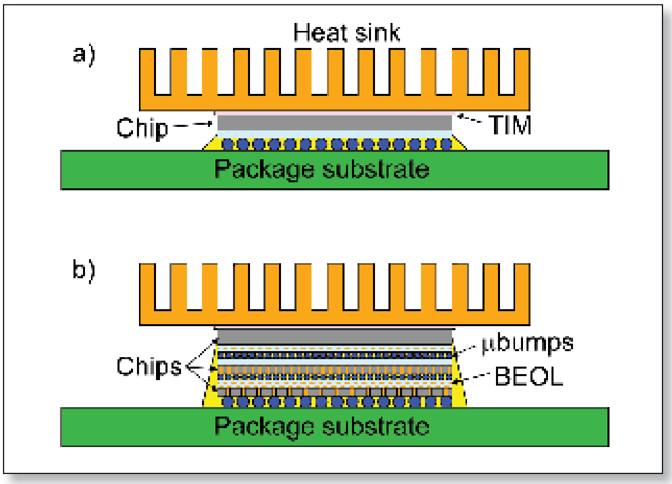

FIGURE 1: Schematic diagram of lid-less chip package (a) and chip stack (b).

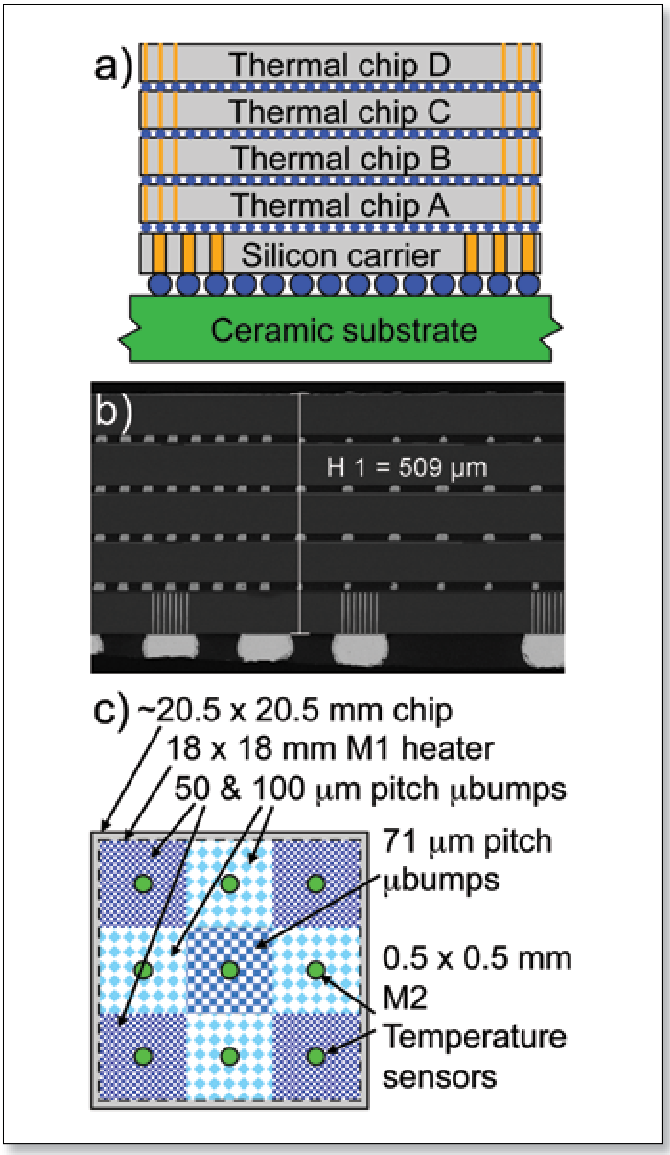

FIGURE 2: Schematic side view (a) and SEM cross section (b) of chip stack test vehicle and thermal chip details (c).

(1) Unit Thermal $R_{th} = \Delta T_{\text{adjacent layers}} * \text{Area}_{\text{Heater}} / \text{Power}$

Note that the values plotted in Fig. 4(c) include the thermal resistance of ~ 5.5 C-mm²/W from the thermal chip. For the underfilled case, if we subtract the contribution from the thermal chip from the average values, for microbump pitches of 50, 71, and 100 μm, the corresponding unit thermal resistances values are 8.0, 15.5, and 19.0 C-mm²/W.

The chip stack was modeled using commercially available thermal simulation software. A conduction model was used which included all components of the package and board. The silicon die and carrier were given default temperature dependent silicon properties and the insulator layers in Table 1 were included. Each of the microbump regions were modeled as homogeneous collapsed cuboids, with effective thru-plane thermal conductivities using a parallel thermal resistance approximation of solder (k = 35 W/m-K), and air or underfill;

(2) $k_{eff} = k_{solder} * (\text{fraction solder}) + k_{air} * (\text{fraction air or underfill})$

Heat transfer coefficient boundary conditions were used to simulate the water cooling and board heat losses. The heat transfer boundary conditions on the bottom of the board were varied from 0 W/m²-K (completely insulated) to 20 W/m²-K to try and determine whether spreading or heat loss through the board was contributing to different resistance values at different layers. We found that the difference in results from varying the heat loss to the board were insignificant and could not explain the differences in resistances at different layers. The spreading was found to be the dominant factor.

The modeled temperature contours, when the bottom chip A was powered are shown in Fig. 5 for the four high chip stack without underfill. The systematic temperature variations in Fig. 5 are roughly consistent with the measured values plotted in Fig. 4(a). At the bottom of the chip stack (chips A & B) the hottest areas are those with the 71 μm and 100 μm pitch microbumps and the temperature distribution is more uniform at the top of the chip stack (chips C & D).

This microbump layer unit thermal resistance includes the contribution from the BLM (ball limiting metallurgy) layers on the chips and intermetallic formation in the Pb-free solder microbumps. The measured values are higher than parallel/series estimates using bulk conductivity values for the solder and underfill. This can be explained by material interfacial resistances, voids, and grain boundary effects. For comparison, with a typical underfilled C4 layer with 200 μm pitch and about 70 μm height, the comparable thermal resistance value is about 100 C-mm²/W. For the 50 μm pitch case, if the unit

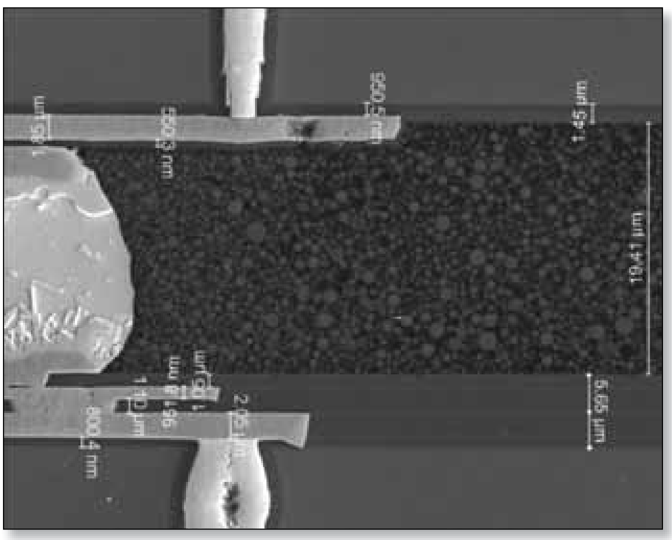

FIGURE 3: Cross sectional SEM image of the insulator and metal layers on the test chips.

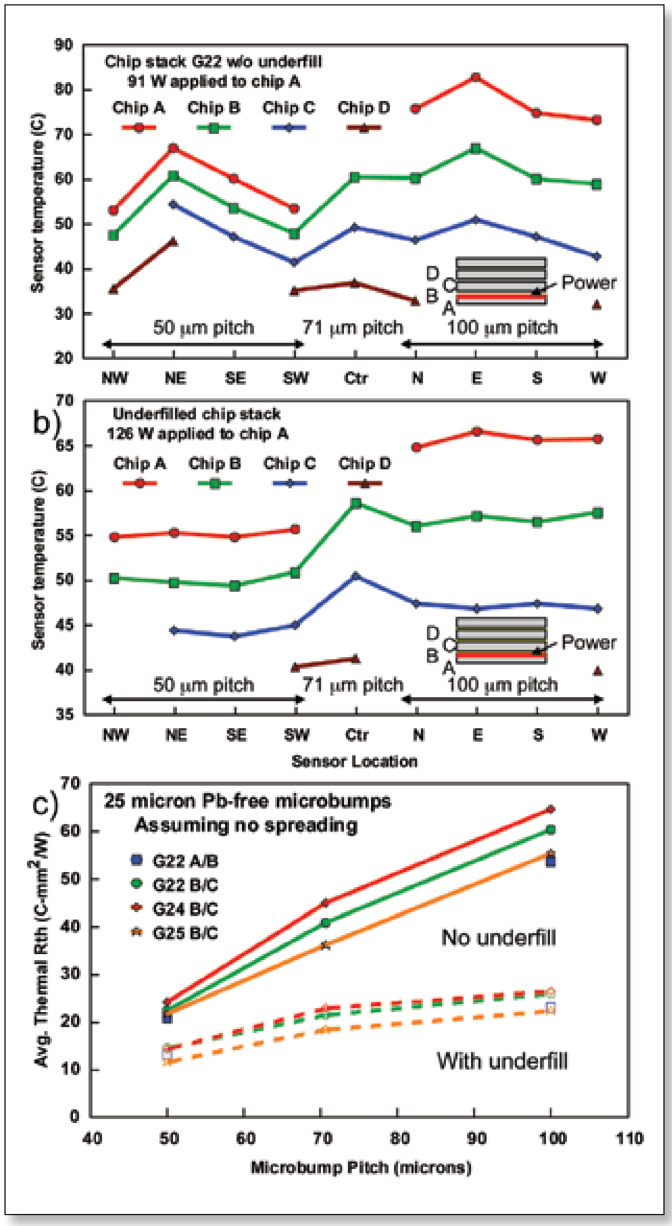

FIGURE 4: Sensor temperature vs. location for chip A powered without (a) and with underfill (b) and average unit thermal resistance values versus microbump pitch (c).

thermal resistance of the microbump layer is assumed to be from two thermal resistance terms in parallel, where the value measured without underfill corresponds to the thermal resistance of the microbumps alone, then the thermal conductance of the underfill can be estimated to be roughly equal to that of the microbumps alone. This estimation ignores the spreading resistance term and the conduction through air in the no underfill case.

Location	Material	Thickness (µm)	k (W/m-K)	R_{th}; C-mm^2/W
Bottom	PECVD SiO_2	0.5	1.1	0.5
	PECVD SiN_x	1	1.5	0.7
Si subtrate	Si	81	117	0.7
Top	Thermal SiO_2	1	1.2	0.8
	PECVD SiO_2	3	1.1	2.7
	PECVD SiN_x	0.2	1.5	0.1
			Total	**5.5**

TABLE 1: Chip insulator layers and thermal resistance values.

CONCLUSIONS

The thermal resistance of Pb-free ~25 µm diameter microbumps with pitches of 50, 71, and 100 µm has been measured with and without underfill in four-layer chip stacks. With underfill, the unit thermal resistance values were 8.0, 15.5, and 19.0 C-mm^2/W for 50, 71, and 100 µm pitch microbumps, respectively. For the 50 µm pitch case, the thermal conduction from the underfill is roughly equal to that of the microbumps alone. In this work, we have experimentally characterized the thermal resistance of Pb-free microbumps in a chip stack, which is necessary for the design of future systems based on 3D chip stacks.

ACKNOWLEDGMENTS

We are deeply indebted to P. Andry, B. Dang, J.H. Magerlein, J. Maria, and R. Polastre for their assistance with this work.

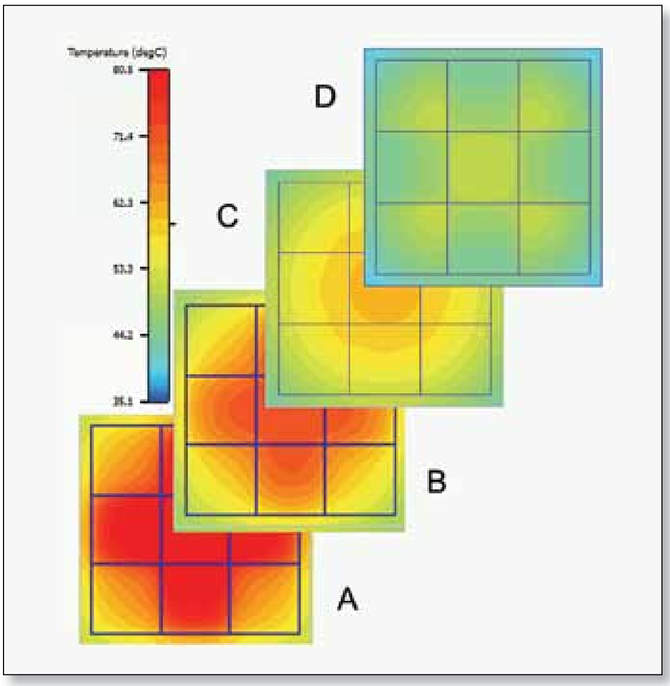

FIGURE 5: Modeled temperature contours with the bottom chip powered in a chip stack without underfill.

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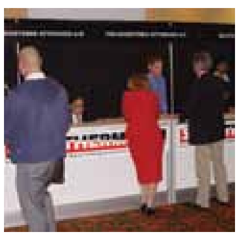

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Advanced Thermal & Environmental Concepts
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Alexandria Industries
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MC-21, Inc. (Metallic Composites for the 21st Century)
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154 Crimson Lane, Elizabethtown, PA 17022, USA; 866-281-0988; Fax: 866-281-0988; www.specsensors.com

Spirig Advanced Technologies Inc., (SAT)
144 Oakland Street, Springfield, MA, 01108, USA; 413-788-6191; Fax: 413-788-910; www.spirig.com; sat@spirig.com

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STEGO, Inc.
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Stockwell Elastomerics, Inc.
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SUNON Inc.
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31 B St., Burlington, MA 01803 USA; 781-272-3969; Fax: 781-272-9185; www.surmet.com

T

TA Instruments
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Temperature@lert
108 Lincoln Street, Suite BA, Boston, MA 02110; 866-524-3540, USA; Fax: 866-415-9884; www.temperaturealert.com

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Thermal Solutions Inc.
3135 S. State St., Suite 108, Ann Arbor, MI 48108, USA; 734-761-1956; Fax: 734-761-9855; www.thermalsoftware.com; GenInfo@thermalsoftware.com

Thermshield LLC
Village West II, Suites 2D/E, 36 Country Club Road, Gilford, NH 03247, USA; 603-524-3714; Fax: 603-524-6602 www.thermshield.com; info@thermshield.com

3M
3M Center, St. Paul, MN 55144-1000, USA; 888-364-3577; www.3m.com/electronics

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35 Old Dock Road, Yaphank, NY 11980 USA; 631-345-6509; Fax: 631-775-4023; info@timtronics.com; www.timtronics.com

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700 Gwanpyeong-dong, Yuseong-gu, Daejeon-si, Korea; +82-31-888-9258; Fax: +82-42-935-3752; www.coolttm.com; ttm@coolttm.com

U

Universal Air Filter Company
Sauget, Ill., USA; 618-271-7300; www.uaf.com

V

Verotec Inc.
33 Bridge St., Pelham, NH 03053, USA; 603-635-5199; Fax: 603-635-5299; www.verotec.us: info@vettecorp.com

Vortec, an ITW Company
10125 Carver Rd, Blue Ash, OH 45242; 513-891-7474; Fax: 513-891-4092; www.itw-air.com

W

Wakefield-Vette
33 Bridge St., Pelham, NH 03076, USA; 603-635-2800; Fax: 603-635-1900; www.wakefield-vette.com

Wavelength Electronics Inc.
51 Evergreen Drive, Bozeman, MT, 59715, USA; 406-587-4910, Fax: 406-587-4911; www.teamwavelength.com; sales@teamwavelength.com

Waypoint Thermal Management, Inc.
150 River Road, Suite I-4A, Montville, NJ 07045, USA; 908-672-7362; Fax: 973-257-8999; www.waypointmanagement.com; sales@waypointmanagement.com

Wolverine Tube Inc. - MicroCool Division
100 Market St. NE, Decatur, AL 35601, USA; 256-580-3530; Fax: 256-580-3502; www.microcooling.com

Y

YS TECH USA
12691 Monarch St., Garden Grove, CA, 92841, USA; 714-379-1400; Fax: 714-379-1010; www.ystechusa.com

Z

Zalman Tech Co., Ltd.
#1007 Daeryung Techno Town III, 448 Gasan-dong, Gumchun-gu, Seoul, 153-803, Korea; +82-2-2107-3232; Fax: +82-2-2107-3322; www.zalman.co.kr

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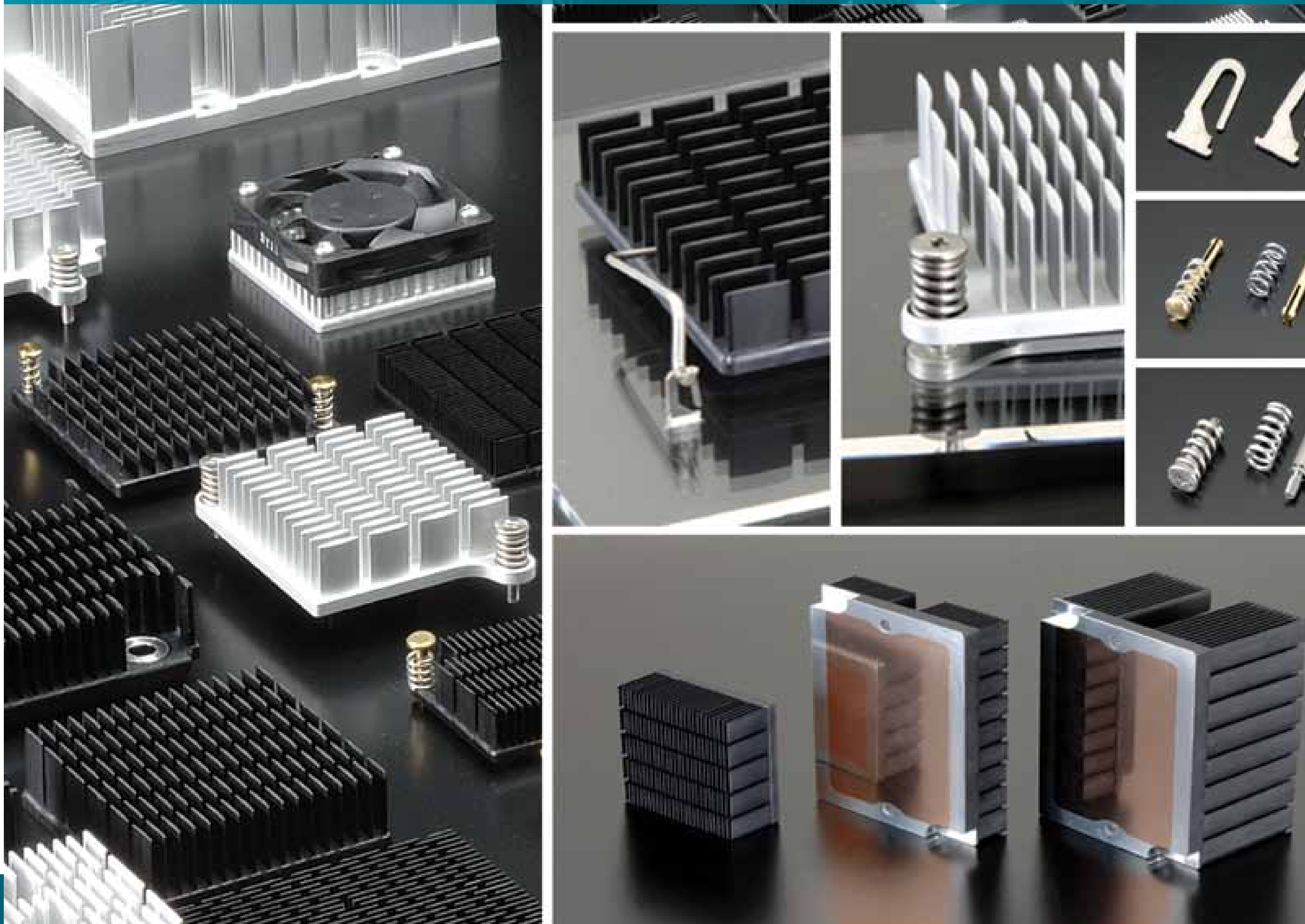
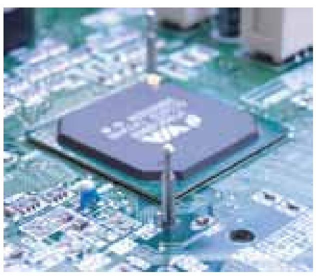


QSZ Clip

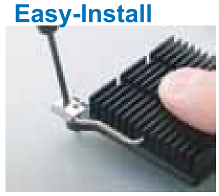
Minimum PCB Area

Pins only require 1.8mm diameter holes in the PCB.



Mounting Security

Easy-Install



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