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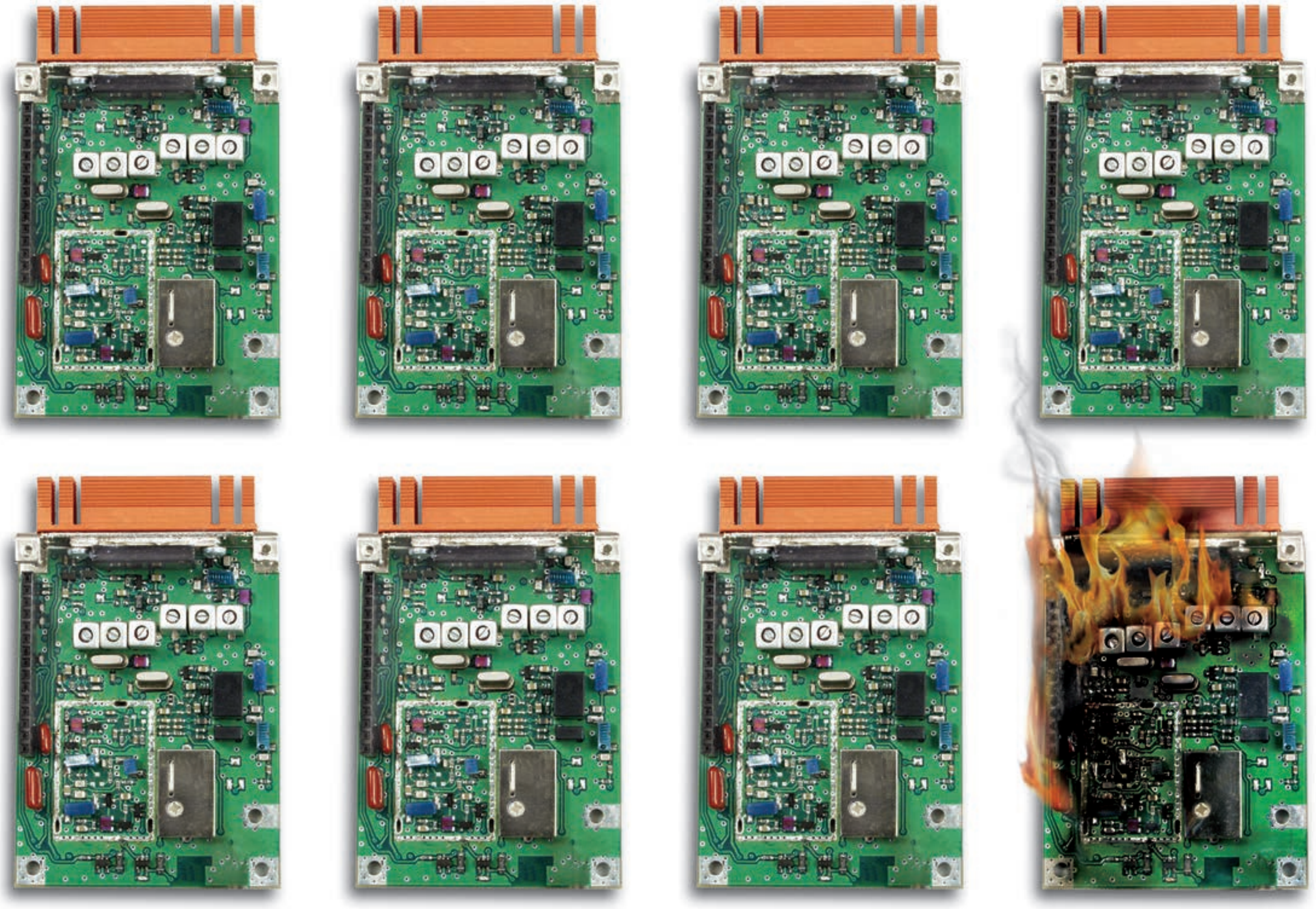

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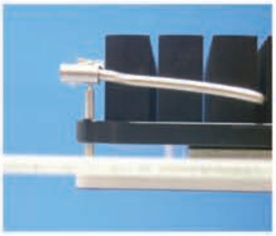

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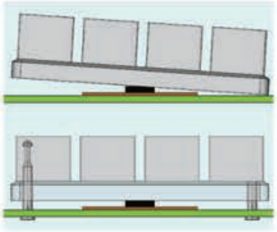

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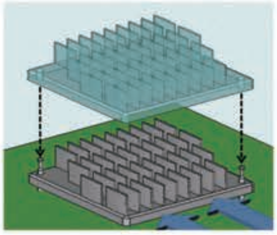

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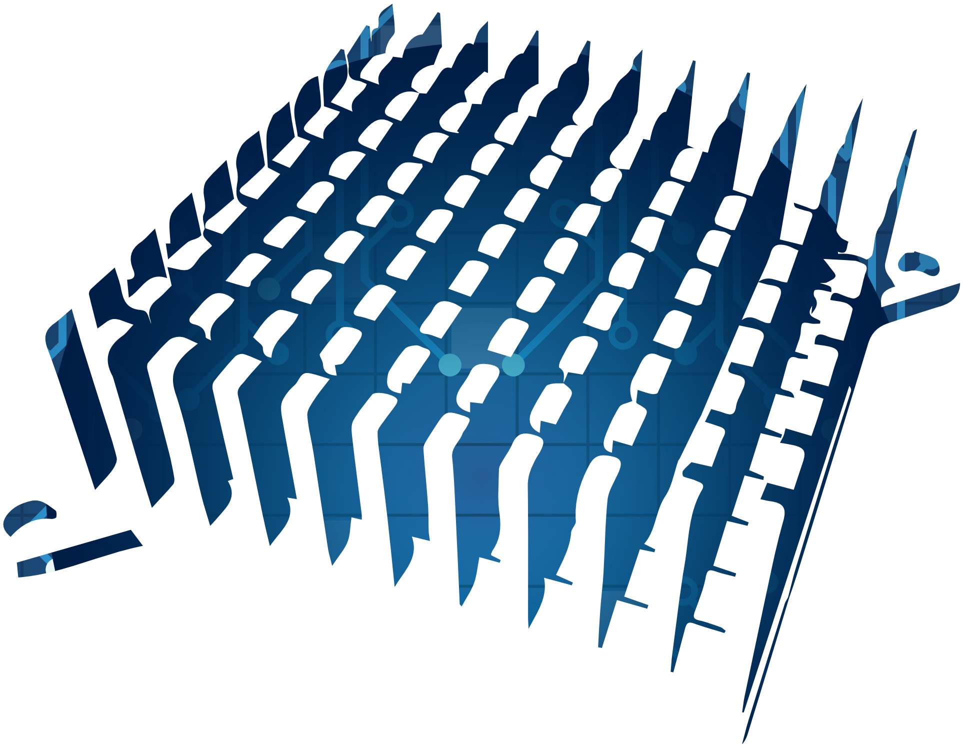

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ITEM MEDIA

EDITORIAL

"It Depends…"

Ross Wilcoxon, Principal Mechanical Engineer / Advanced Technology Center

A few months ago, while I was uncharacteristically checking my work email on a Friday evening, I found a message from Bruce Guenin. He was inquiring whether I would be interested in joining the editorial board for *Electronics Cooling* magazine. I gave what I hope was a professional response and said that I was pleased with the invitation, but I needed to check with my boss to make sure that my company was OK with my committing to another outside activity. My answer was a lie of course – I wasn't just pleased with the invitation, I was ecstatic with it. And regardless of what my boss said, I had no intention of turning down the invitation (sorry Anna…).

The reason that I was so happy and felt so honored for being asked to become part of *Electronics Cooling* stems from the deep respect that I have for the publication. This magazine serves a unique role in our industry – somewhere between a technical journal and a trade magazine. As I thought about how to describe what ECM does, I thought of the answer that my co-worker Doug Pauls gives to virtually any engineering question. That answer is "It Depends". I call this the Pauls Principle and have even slightly formalized it by making the observation that , if the equation that is related to a question as to whether some change will make a difference has a plus (or minus) sign in it, the answer is always 'It Depends'. In other words, if A+B=C, you need to know what the magnitude of A is in order to determine if changing B will have a significant impact on C.

The role of engineers is often to gather information, through research, analysis, simulation, etc. to convert the situation from 'It Depends' to something less ambiguous. Over its history, *Electronics Cooling* has striven to meet the needs of its readers to better understand all facets of electronics cooling technologies. The editors have worked hard to avoid commercial articles, which may not provide a sufficiently unbiased perspective to better answer the 'It Depends' question. *Electronics Cooling* editors have also assisted numerous authors of journal and conference papers to distill them into articles that highlight the critical technical issues with less focus on the specific details. These articles make the information more accessible to the practicing engineer who may have a broader (and shallower) knowledge base than the academics and other experts for which they were initially written. Finding the middle ground to ensure that information is neither biased or inaccessible to non-experts is critical in providing engineers the tools to come up with answers that are more useful than 'It Depends'.

Electronics Cooling magazine is undergoing some significant changes this year. So far this year we have two new editors (Victor Chiriac of Qualcomm and myself). More changes are coming; starting in 2017 ECM will have a permanent editor (MP Divakar) and each issue will be dedicated to a specific theme. There are also plans to grow the editorial staff, in part to increase the range of topic articles to topics beyond that of the current editors (who will remain part of the magazine's editorial staff). These changes will allow the publisher to better respond to evolving market conditions and to provide readers with a better focus on critical trends in our industry. In a few months' time, will you consider all of these changes to be improvements? Given the rest of this editorial, I feel like I would sound hypocritical to say anything other than 'It Depends'. But I have very high hopes and am confident that you will continue to consider *Electronics Cooling* magazine to be a valuable addition to your mail/inbox.

Finally, I would like to acknowledge and thank two individuals who have made significant contributions to *Electronics Cooling* magazine in recent years. Jim Wilson, who stepped down as an editor earlier this year, and Peter Rodgers, who is stepping down after this issue, have both done a fantastic job of ensuring that this magazine addressed topics ranging from future technologies to information that can be directly used by the practicing thermal engineer, such as material properties. Their dedication, as well as that of the other members of the editorial staff, ensured that *Electronics Cooling* magazine continued in its goal to convey practical and current information to the thermal community in the electronics industry.

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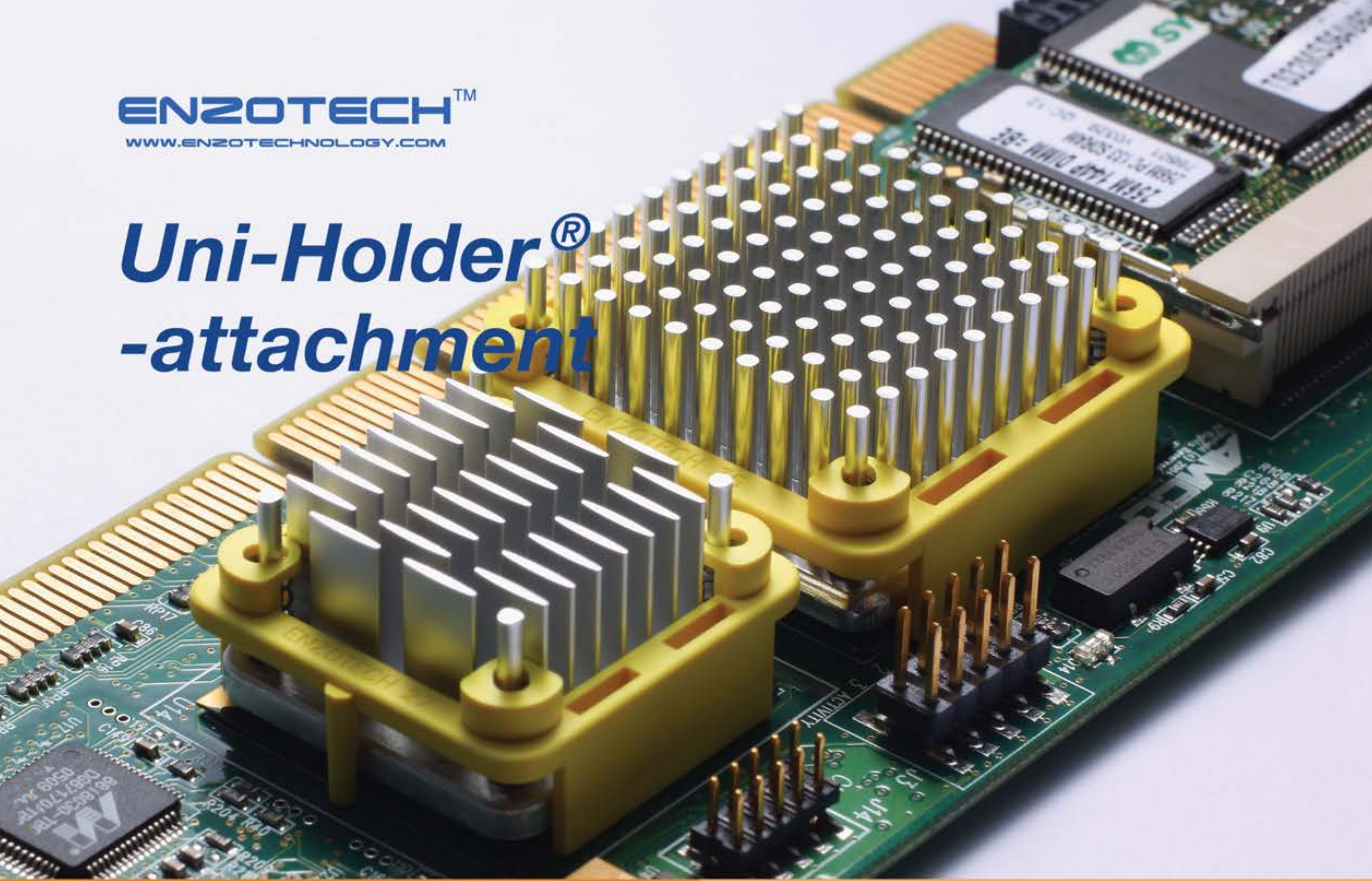

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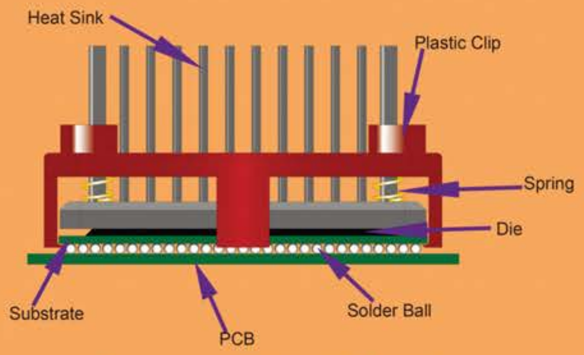

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COOLING EVENTS

News of Upcoming Thermal Management Events

1ST ETA CONFERENCE 2016

December 1 (Thursday) - 2 (Friday)
Ellington Hotel Berlin / Berlin, Germany

IAV's first Energy and Thermal Management, Air Conditioning, Waste Heat Recovery conference will bring together experts from research and development and from various fields (transport, industry and building engineering) to discuss the latest technological developments and applications for energy efficiency. ETA 2016 will expand the range of topics at the previous IAV thermoelectrics conference and focus on the main topic areas of energy and thermal management, air conditioning, and waste heat recovery. The conference is aimed at representatives of the international automotive industry, academic experts and professionals in industries – such as household appliances, rail or aerospace – that also benefit from efficient energy use.

WEBINAR SERIES – REQUIREMENTS FOR INTERNATIONAL APPROVAL PRODUCT SAFETY: ROUTES TO COMPLIANCE

December 13 (Tuesday) 1:00 Pm - 2:00 Pm
Online

This webinar series will present details on test and evaluation methods for the more common tests required for international approval. The discussion will address test and evaluation methods along with approaches to incorporate safety control measures into your design. This multi-part series of one-hour webinars, presented at regular intervals throughout the calendar year, provides detailed focus on evaluating products, mitigating issues, documentation and understanding the reason for the requirements.

THERMAL DESIGN & COOLING OF ELECTRONICS WORKSHOP

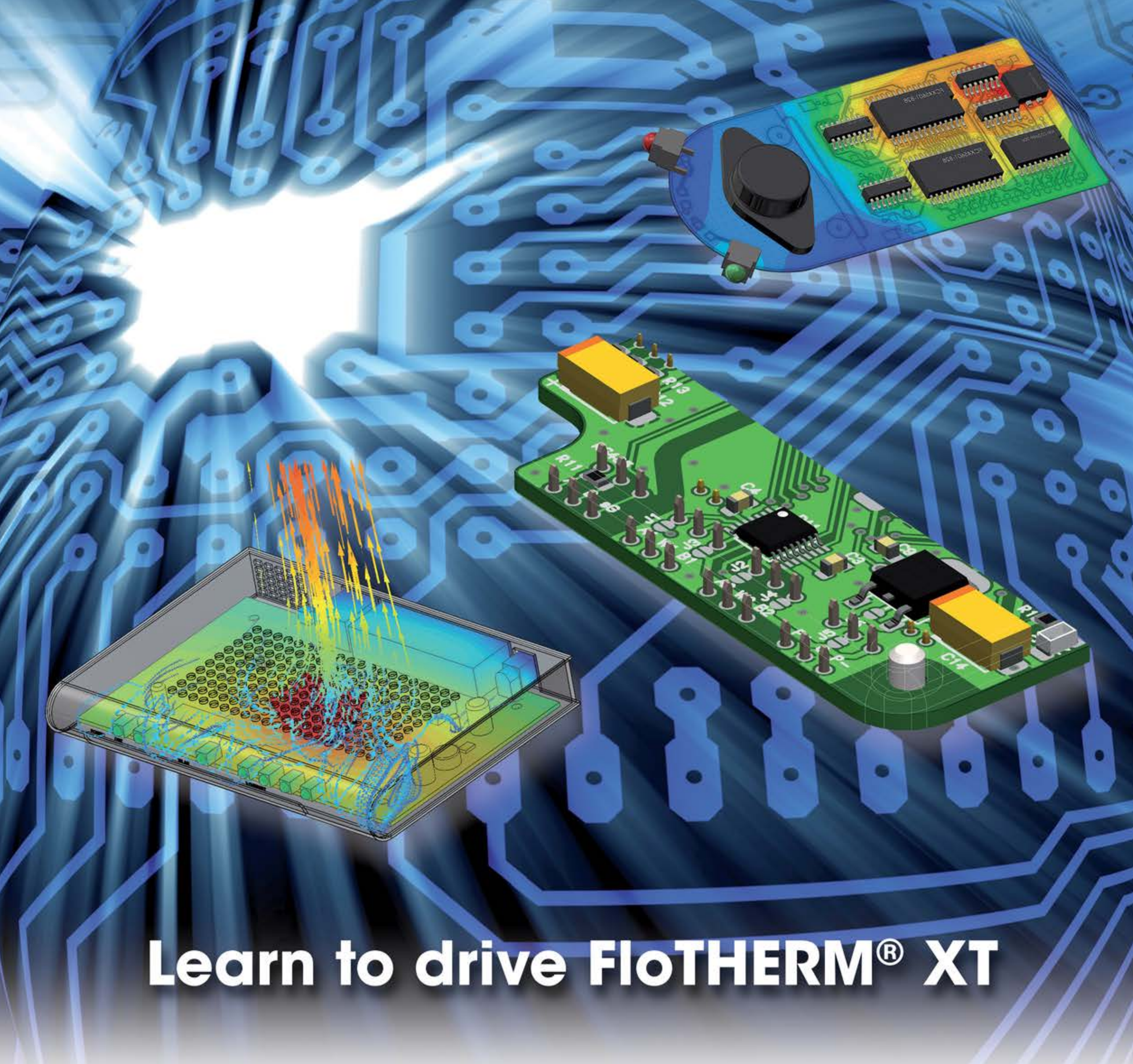
January 5 (Thursday)
Eindhoven, the Netherlands

Experienced lecturers Wendy Luiten (winner of the Prestigious Harvey Rosten Award 2014) and Clemens Lasance (SEMI-THERM THERMI Award winner in 2001) teach the participants how to solve the thermal problems they encounter during all levels of the product creation process. They discuss the why, what and how of thermal management. The course is a balanced mixture between theory and practice. A real-life case obtained from the participants themselves and prepared by the lecturers is used to demonstrate the application of the course principles. Because early knowledge of thermally related problems is imperative to prevent expensive redesigns and a delayed market introduction, thermal design should be part of the product design process from the early start.

DESIGNCON 2017

January 31 (Tuesday) - February 2 (Thursday)
Santa Clara Convention Center / Santa Clara, California

DesignCon, the premier conference for chip, board, and systems design engineers; returns to Silicon Valley for its 22nd year. DesignCon serves the high speed communications and semiconductor communities offering state-of-the-art design methodologies, applications, technologies, and unparalleled networking opportunities. Taking place annually, DesignCon remains the largest gathering of chip, board, and systems designers in the country. Combining technical paper sessions, tutorials, industry panels, product demos, and exhibits; DesignCon brings engineers the latest theories, methodologies, techniques, applications, and demonstrations on PCB design tools, power and signal integrity, jitter and crosstalk, high-speed serial design, test and measurement tools, parallel and memory interface design, ICs, semiconductor components, and more.



Estimating Temperatures in an Air-cooled Closed Box Electronics Enclosure

Robert E. Simons
Associate Editor, IBM Corporation

Editor's note: This is another in a series of reprints of Bob Simons' timeless Calculation Corner columns. Bob served as an Associate Technical Editor of this publication from January, 2001, to December, 2011. For those readers who find this sort of tutorial useful, please refer to the list, compiled by Bob, of other Calculation Corner columns authored by him as well as by others: https://www.electronics-cooling.com/2011/09/a-useful-catalog-of-calculation-corner-articles/

INTRODUCTION

In the majority of air-cooling applications, openings or vents are provided in the enclosure or box in which the electronic components are housed. The required cooling air is drawn in from outside the box by fans or blowers. In some applications however, there may be airborne particulates or other substances in the air that would be injurious to the electrical components in the box and it is necessary to totally seal the box. In such cases a closed-box cooling approach similar to that shown in *Figure 1* may be used. The heat picked up by the air circulating over the components is rejected to outside air via the air-to-air heat exchanger mounted in one of the walls of the box. Unfortunately, a temperature penalty equal to the difference between the temperature of the air exiting the hot side of the heat exchanger ($T_{h\text{-}out}$) and the temperature of the outside air ($T_{c\text{-}in}$) entering the cold side of the heat exchanger is incurred. Consequently, the temperature of components within the box will be higher than if they were directly cooled with outside air.

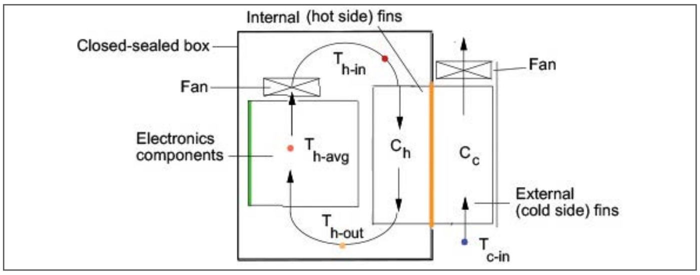


Figure 1. Closed box air-cooling configuration with with double-sided heat sink air-to-air heat exchanger.

The increase in the temperature of the air entering the electronics section (with reference to the outside air temperature) may be calculated using the following equation:

$$T_{h\text{-}out} - T_{c\text{-}in} = q_L\left(\frac{1}{\varepsilon \cdot C_{min}} - \frac{1}{C_h}\right) \tag{1}$$

where q_L is the total heat dissipation within the box,   is the effectiveness of the heat exchanger, and C_{min} is the smaller of the inside (i.e. hot side) air heat capacity rate (C_h) or the outside (i.e. cold side) air heat capacity rate (C_c). *Equation 1* is similar in form to that given in an earlier article addressing a water-to-air hybrid cooling system [1]. In the system under consideration here, the water loop has been replaced with an internal air flow loop and a double-sided heat sink is used instead of a water-to-air finned tube heat exchanger.

The air heat capacity rates in *Equation 1* are readily calculated and are equal to the products of the mass flow rate (m x c_p) and specific heat for each air stream or

$$C_h = \dot{m}_h \times c_p = \rho \times V_h \times c_p \tag{2}$$

and

$$C_c = \dot{m}_c \times c_p = \rho \times V_c \times c_p \tag{3}$$

where p is the density of air and V_h and V_c are the volumetric air flow rates on the hot and cold sides of the heat exchanger respectively.

In some cases the average air temperature through the electronics section, $T_{h\text{-}avg}$, is used as the reference temperature. Then the average cooling air temperature through the electronics section is given by,

$$T_{h\text{-}avg} = T_{c\text{-}in} + q_L\left(\frac{1}{\varepsilon \cdot C_{min}} - \frac{0.5}{C_h}\right) \tag{4}$$

HEAT EXCHANGER EFFECTIVENESS

For *Equations 1* and *4* to be useful the effectiveness, ε, must be known. Heat exchanger effectiveness is the ratio of the actual heat transfer rate of a heat exchanger to the thermodynamically limited maximum possible heat transfer rate in a heat exchanger of infinite area. It is a function of heat exchanger geometry, structure, and the hot and cold side air flow rates. Values of effectiveness for heat exchangers may sometimes be found in vendor literature. For the purposes of this Calculation Corner, a double-sided counter-flow heat sink heat exchanger as shown in *Figure 2* will be considered and a procedure to estimate effectiveness will be outlined.

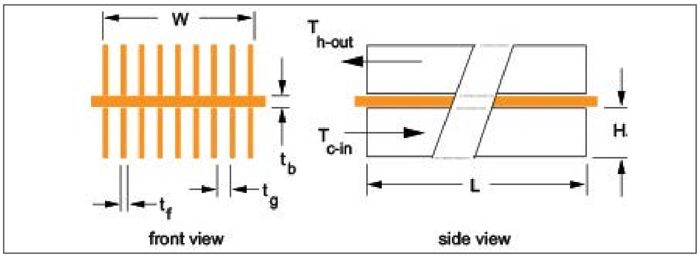


Figure 2. Double-sided heat sink used as counter-flow heat exchanger.

For a counter-flow heat exchanger, effectiveness is given by,

$$\varepsilon = \frac{1 - e^{-NTU \cdot (1 - C_r)}}{1 - C_r\, e^{-NTU \cdot (1 - C_r)}} \tag{5}$$

where Cr is the ratio of air flow heat capacity rates given by,

$$C_r = \frac{C_{min}}{C_{max}} \tag{6}$$

or,

$$C_r = \frac{C_c}{C_h} \text{ for } C_c < C_h \text{ and } C_r = \frac{C_h}{C_c} \text{ for } C_h < C_c$$

Comparable formulas for effectiveness of other heat exchanger configurations and types may be found in references [2] and [3].

DETERMINING NTU

The term, NTU, in *Equation (5)* is a widely used dimensionless parameter called the number of heat transfer units. It is a measure of the heat transfer size of the exchanger, the greater the number of NTUs the closer the heat exchanger approaches the thermodynamic limit. The number of NTUs is given by,

$$NTU = \frac{U \cdot A}{C_{min}} \tag{7}$$

where U is the overall unit thermal conductance of the heat exchanger and A is the area. For the double-sided heat sink heat exchanger U•A is given by,

$$UA = \frac{1}{R_h + R_b + R_c} \tag{8}$$

where R_h and R_c are the convective thermal resistances on the hot side (inside the box) and cold side (outside the box) respectively of the double-sided heat sink and R_b is the thermal conduction resistance across the base of the heat sink.

The convective thermal resistance on each side of the heat sink heat exchanger is a function of the convective heat transfer coefficient, fin surface area, and fin thermal efficiency. For the purposes of this analysis, fully developed laminar flow and heat transfer is assumed. Under this condition the Nusselt number is a function of the flow passage geometry between the fins. As shown in *Figure 3*, an equation relating Nusselt number to aspect ratio was fitted to values of Nusselt number presented in reference [4]. This equation is

$$Nu = 11.24 \cdot (t_g / H_f)^{1.22} - 15.83 \cdot (t_g / H_f)^{0.83} + 8.24 \tag{9}$$

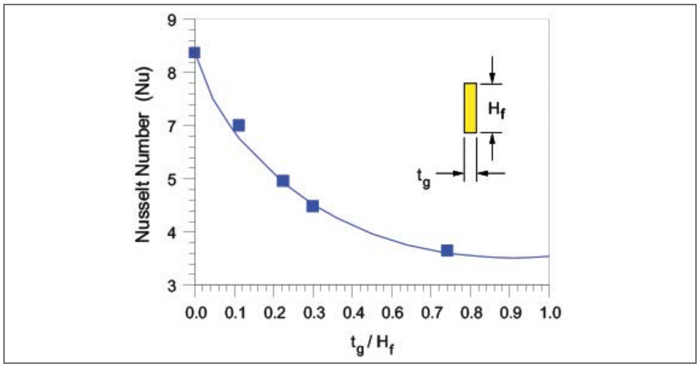


Figure 3. Laminar Nusselt number versus flow passage aspect ratio (adapted from [4]).

The heat transfer coefficient, h, acting on the fins is then calculated from,

$$h = Nu \frac{k_{air}}{D_h} \tag{10}$$

The heat transfer coefficient, h, acting on the fins is then calculated from,

$$D_h = 2 \frac{(t_g \cdot H_f)}{(t_g + H_f)} \tag{11}$$

The convective thermal resistance, R, on each side of the heat sink is given by,

$$R = \frac{1}{h \cdot (\eta_f \cdot A_f + A_b)} \tag{12}$$

where A_f is the lateral surface area of all the fins on the heat sink side being considered, A_b is the exposed base area on that side, and η_f is the thermal efficiency of the fins. The thermal efficiency of the fins is given by,

$$\eta_f = \frac{\tanh(m \cdot H_f)}{m \cdot H_f} \tag{13}$$

where m is given by

$$m = \sqrt{2 \frac{H_f}{k_f \cdot t_f}} \tag{14}$$

and k_f is the fin thermal conductivity.

The conduction thermal resistance across the base is given by,

$$R_b = \frac{t_b}{k_b \cdot W \cdot L} \tag{15}$$

The foregoing equations may be readily automated using mathematical software such as Mathcad® or MATLAB® or any of the common spreadsheet programs. If the reader chooses to automate these calculations, one word of caution is order. When the air heat capacity rates of the hot and cold flow streams are equal, C_r is equal to 1. Examination of *Equation 6* shows that this will cause the exponents of the exponential terms in the numerator and denominator to go to zero with an overall result of zero divided by zero. To avoid this difficulty, set C_r to 0.999 or 1.001 for C_r equal to 1.

EXAMPLE CALCULATIONS

To illustrate the application of these equations calculations were performed for an aluminum double-sided heat sink with the following dimensions:

Width (W) = 150 mm
Length (L) = 150 mm
Base thickness (tb) = 5 mm
Fin height (Hf) = 25 mm
Fin thickness (tf) = 1.5 mm
Fin gap (tg) = 2.3 mm
Number of fins = 40

Applying *Equations 8–15,* it was found that these dimensions result in a convective thermal resistance of 0.083 °C/W on each side of the heat exchanger and an overall unit thermal conductance of 6.0 °C/W. Further calculations revealed that increasing the fin height on both sides of the heat exchanger to 70 mm would approximately double the unit thermal conductance.

Equations 1-7 were then applied to determine the effectiveness and the increase in the temperature of air entering the electronics section above the temperature of the outside air entering the cold side of the heat exchanger. Air flow rates of 25 (0.0118 m^3/s) and 50 (0.0236 m^3/s) CFM were used on the hot side of the heat sink and flow rates ranging from 5 (0.0024 m^3/s) to 70 (0.0330 m^3/s) were used for the cold side. The effects of flow rate and overall thermal conductance on the calculated heat exchanger effectiveness are illustrated in *Figure 4*. The corresponding increase in the temperature of air entering the electronics section above the temperature of the outside air is shown in *Figure 5* for the same conditions.

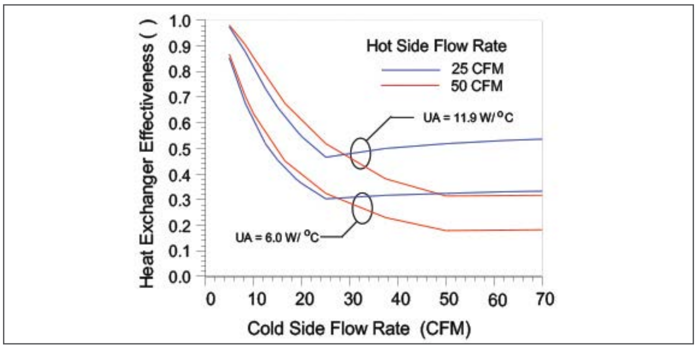


Figure 4. Effect of flow rates and UA on double-sided heat sink counter-flow heat exchanger effectiveness.

It may be noted from inspection of *Figure 5* that the air entering the electronics section is actually cooler with a lower flow rate through the hot side of the heat exchanger. Although these results may seem counter-intuitive, they may be understood by examining *Figure 6. Figure 6* shows the temperature increase above ambient (i.e. temperature of air outside the enclosure) for: 1) the air entering the electronics section ($T_{h\text{-}out} - T_{c\text{-}in}$); 2) the average air temperature in the electronics section ($T_{h\text{-}avg} - T_{c\text{-}in}$); and 3) the air leaving the electronics section and entering the hot side of the heat exchanger ($T_{h\text{-}in} - T_{c\text{-}in}$). For low air flow rates within the enclosure, the temperature rise of the air passing over the heat dissipating electronics will be the greatest resulting in the highest inlet air temperatures to the hot side of the heat exchanger. Conversely, the combination of a high temperature difference ($T_{h\text{-}in} - T_{c\text{-}in}$) and low air heat capacity rate at the low flow will result in the greatest reduction in the temperature of the warm air passing through the hot side of the heat exchanger. As the hot side air flow rate is increased, these two effects are reduced. This results in an increase in the temperature of the air entering the electronics section and a reduction in the temperature of the air entering the hot side of the heat exchanger. As one might expect, the average cooling air temperature within the electronics section decreases with increasing air flow in the box.

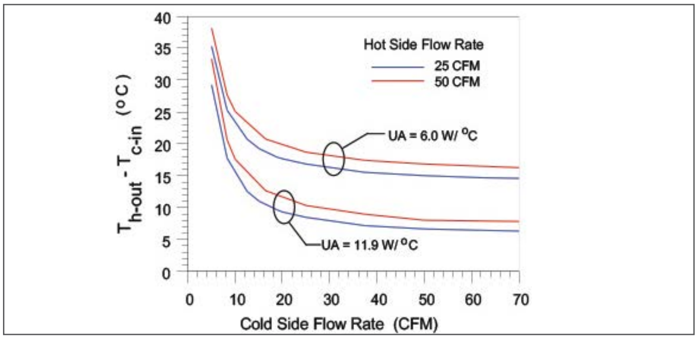


Figure 5. Temperature increase of cooling air entering electronics section above external air temperature.

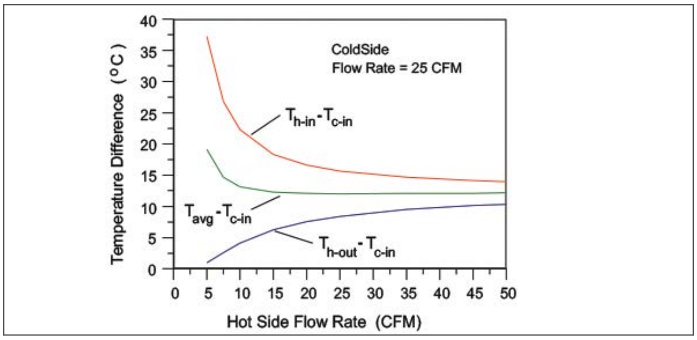


Figure 6. Effect of hot side air flow rate on air temperatures within closed box.

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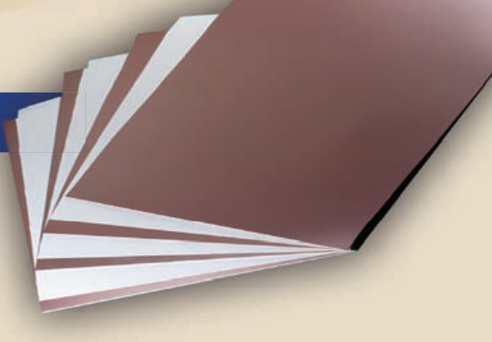

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7 years of college down the drain …might as well join the Peace Corps…

John "Bluto" Blutarsky[1]

Ross Wilcoxon
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I would hazard a guess that the majority of people bothering to read an article on electronics cooling likely work in the electronics industry. Moreover, it is probably a pretty good bet that a lot of them have actually taken a class on heat transfer at some point. Since most of us eventually graduated, it seems reasonable, therefore, to believe that most of us at some point actually understood fundamental heat transfer analysis well enough to pass a class on the topic.

But thanks to the availability of powerful analysis software, a lot of people have had the luxury of forgetting, or at least ignoring, their hard-won thermal management education. Just fire up the computer, open the finite element modeling tool and generate some CFD (color, for directors). And the analysis tools generally work so well that these people often get away with it and produce sufficiently accurate results. Most commercial tools have been validated well enough that they don't have too many bugs. As long as the user is entering reasonable inputs the software will usually output reasonable results. Ignoring the two caveats in the preceding sentence is what can occasionally lead to heartache, gnashing of teeth, wearing of sackcloth, and most importantly, panicked redesigns after an initial qual test failure.

These two caveats are not necessarily unrelated, but I will talk about them separately. Let's start with the second caveat: 'will usually'. While the vast majority of commercial software works as advertised, versions do sneak out that don't have all the bugs worked out. Take some comfort if the version number of whatever you're using is in the double digits; that improves the odds that someone else has already discovered most of the bugs that once existed. But even well-established and respected analysis tools can have undiscovered features, particularly in areas that only a small portion of the users exercise.

In a fairly well-known case a few years ago, the maker of a widely-used finite element analysis tool had implemented an incorrect creep equation for analyzing solder joint fatigue. Eventually, it was recognized that the equation had not been correctly coded – which led to a number of investigations that had to be repeated. A more likely problem than the software getting things wrong is the user getting things wrong with unreasonable inputs. Sometimes it's a matter of the user doing something silly and the software not being responsible enough to be the grown-up and tell them so.

A few years ago I was in a design review being presented by a very young engineer who proudly showed us his free convection box that featured a lot of horizontal fins. I asked why the fins were oriented that way and he naively asked 'it makes a difference?' Apparently not to the software, which allowed the user to select a 'free convection' boundary condition option and didn't bother mentioning that making the plate fins run perpendicular to gravity would have a less than desirable effect on their natural convection performance. Similarly, if things are too easy it can be easy to make a dumb error with units or materials; despite the similarity in their names, alumina and aluminum have very different properties if you choose the wrong option on a pick list (likewise silicon and silicone).

Even when the inputs are correct and the software does what it is supposed to, if you are asking it to solve the wrong problem you can produce some poor results, or at a minimum hurt your credibility. One analysis approach that has made me pull out what little hair I have left is when the analysis of something operating at extremely high altitude is assumed to have no radiation. Granted, radiation is tricky because you need to know the temperatures of nearby equipment to account for radiation exchange between units. In most cases, there will likely be a net heat loss by radiation, so ignoring radiation can provide some measure of conservatism while also making the analysis a lot easier. But when things are operating at a 20 km pressure altitude, there aren't many ways to remove heat other than with radiation.

In another design review of the previously mentioned horizontal fin box, which happily had been modified by that point to have its fins pointing in the right direction, its performance at altitude was shown. For that analysis, radiation was ignored and the design review showed extremely precise temperatures (reported to 4 or 5 decimal places) that were high enough that the system would have stopped working about 100 degrees earlier because all the components would have de-soldered themselves.

As I recall, the main point of the analysis had been to convince management that a fan was really needed for the design, which I guess is what it did. However, I thought that this was accomplished at a costs of some of the analyst's credibility.

Because of these potential pitfalls, I am a big believer in doing some level of first-order analysis before, or in parallel with, running analysis tools. By first-order analysis, I mean you should actually dig out your undergraduate heat transfer book, but you probably don't need to go past the first couple chapters. You can do a lot of sanity checks by just using one-dimensional heat transfer equations for conduction and convection. These sanity checks won't be sufficiently accurate to replace modeling, but they will give you a starting point and something to compare against more detailed analyses.

The goal is to get into the ball park of the right answer; just getting into the right Zip Code might be good enough. Even if the sanity check doesn't agree with other analysis, if it is done correctly it should provide insight into understanding the system, such that the physics of the problem can be used to explain why things don't match. For example, if an initial estimate under-predicts the temperature of a finned heat sink compared to CFD analysis, the difference may be due to your not including fin efficiency or latent heating effects of the air. But if you instead over-predict temperatures with your first order estimate, try to figure out what you missed – or more importantly if you might have missed something in the computer-based analysis.

My main point is that you probably spent at least some time learning a few things in college, so you might as well try to use them once in a while. You usually don't have to go into a lot of depth or drag out the really complex correlations, many of which are essentially buried into the software tools that you are using. But having an independent method to double check results to see if the results have the right order of magnitude can save you some embarrassment and credibility. A few years ago I was at a status review meeting at which two different excessively educated engineers (i.e. PhD's) showed results from their detailed CFD analyses. They showed temperatures that were many tens of degrees cooler than my spreadsheet analysis had predicted.

Their results were quite impressive looking and included some cool animations that showed the fluid flow patterns inside and outside the system. But a simple calculation using the surface area and power dissipation showed that, in order to maintain their predicted surface temperature, the convection coefficient had to be about 10-100 times what could reasonably expected with air cooling. It turned out that the analysis was based on a newly released piece of software that, for some reason, did not play well with the symmetry boundary condition that had been used to simplify the analysis.

That review didn't exactly leave me terribly interested in getting my own copy of that software or with a lot of confidence in any of their subsequent calculations. They could have easily avoided that result by investing thirty seconds into a sanity check.

Keep in mind that in this short column I have used up most of the examples of computer modeling gone wrong that I have encountered over the past two decades. In the vast majority of cases, the analysts and the software perform extremely well. But it only takes one outlier in the distribution of analysis results to create some problems. So I suggest that people make a habit of maintaining some level of skepticism about the infallibility of analysis software and try to put their education to work once in a while.

REFERENCES

[1] Fans of the movie "Animal House" will undoubtedly note that I have edited this quote to make it more suitable for use in *Electronics Cooling®* Magazine

Case Study: Thermal Design and Analysis of a Combat-Ready Electronics Unit

Jim Smith,
Lead Mechanical Engineer

INTRODUCTION

Militaries continue to expand their use of electronics in harsh environments while preserving an absolute minimal risk of failure. In this regard, effort spent early in the design process on concept development, parametric and trade-off studies, and simulation-driven design can yield amplified benefits in terms of product performance and reliability, reduced development costs, shorter overall design schedules, and minimized redesign iterations. This article describes a portion of the thermal management development process and highlights a few design elements of an electronics unit that is part of a deployed defense system.

The electronics unit under consideration is part of a surveillance system that detects hostile troop movements at long distances. The unit is used in three system configurations that are tailored for the expeditionary setting.and the selection of sensors desired. The three variants (A, B, & C) of the electronics unit are identical except in how they are used and physically mounted, as shown in *Table 1*. Due to the different combination of sensors and cameras selected, each configuration dissipates a different amount of power and has a different orientation relative to gravity.

Table 1: Design options for a surveillance system electronic unit

Configuration	Total Peak Internal Power Dissipation (W)	Characteristics
A	137	Lightweight. Carried via backpack and simply set up at ground level.
B	102	Capability and mobility are a blend of Configurations A and C
C	88.6	Mounted with a suite of sensors and cameras on a telescoping, self-erecting, 33m high trailer-mounted tower to provide enhanced “beyond-the-fence” observational capabilities.

The functional design objective for the electronics unit was to develop a Versa Module Eurocard (VME) enclosure/chassis that would integrate the Intelligence/Surveillance/Reconnaissance (ISR) sensor data into a single Ethernet line. The unit is tasked with video processing, sensor input/output signal conditioning and processing, and sensor/camera power distribution and control. The unit utilizes both Commercial-Off-The-Shelf (COTS) and custom-designed Circuit Card Assembly (CCAs). Because of the high-mobility requirements, the size and weight (13.6 kg, max.) is an imposed design constraint.

Exterior views of the electronic unit are shown in *Figure 1*. The nominal outside dimensions of the unit are 27.3 cm wide x 21.6 cm high x 27.9 cm long.

Inside, there are four VME CCAs: a custom relay CCA and three COTS CCAs that support I/O, Video Encoding, and Ethernet functions. These VME CCAs are mounted directly to slots in the chassis side walls. A power supply CCA utilizes an assortment of DC-DC converters and filters that are mounted directly to the chassis bottom panel. The chassis is fabricated from machined aluminum panels of Alloy 6063-T52 (thermal conductivity of 209 W/mK). Fins are incorporated into the top, bottom, and side panels. The front and back panels are removable for servicing, or future configuration changes or upgrades.

Figure 1: Front and rear views of unit.

The primary internal thermal loads, given in *Table 1*, are generated by the VME CCAs, and the DC-DC converters. The unit is subjected to an external solar thermal load, also. During maximum solar exposure [1], the units can be subjected to an additional 80.4 W for a two-hour time period. This period is considered sufficiently long to permit steady state thermal analysis to be employed.

Jim Smith

Jim is the Lead Mechanical Engineer at Sechan Electronics where he has worked for sixteen years, developing electronics defense systems. He earned a BSME from Lehigh University in 1980, and a MSME from the Georgia Institute of Technology in 1983. He is a registered Professional Engineer in Pennsylvania. Jim’s prior experiences include development of medical products, and design and optimization of industrial products and systems.

The operating temperature limits, established by MIL-HDBK-310 [2], are a minimum and maximum ambient temperature of -32°C, and +49°C, respectively. The upper operating temperature limit applies concurrently with the solar radiation exposure. Other environmental considerations that contribute to the thermal management challenges include Electromagnetic Interference (EMI), altitude, rain, freezing rain, sand and dust, Nuclear/Biological/Chemical (NBC) exposure, shock, and vibration requirements as per MIL-STD-810 [3].

APPROACH

After initial hand calculations and spreadsheet analyses had been used to establish an initial design, a detailed thermal model was generated to perform CFD thermal analysis.

The CFD analysis included the effects of radiation with the painted aluminum chassis exterior assigned an emissivity of 0.92, while the interior chemical-conversion coated aluminum surfaces were assigned an emissivity of 0.20. The VME CCAs are conduction-cooled and rely on an intimate metal-to-metal interface to the chassis slots that is achieved using Wedge-lok connectors. An estimated Wedge-lok contact resistance of 1.1 °C -cm^2/W [4] was incorporated into the analysis model. System temperature design requirements were established by the COTS VME CCAs (with maximum allowable card-edge continuous operating temperature of 85°C), the DC-DC converters (maximum allowable baseplate temperature of 100°C), and the Relays (maximum allowable case temperature of 100°C).

The initial CFD model was run for the three thermal load scenarios with and without solar loading. Initially, the maximum internal power dissipation was estimated to be 153 W. However, detailed evaluation of the electrical design eventually reduced the maximum load to 137 W. The initial results without solar loading indicated that the VME card edges could reach 92.4°C (7°C above their limit) while the DC-DC converters could reach 95.8°C (4°C below their limit).

To reduce the temperature of the VME CCAs, the internal chassis design was modified to allow the fin lengths to be increased from 1.01 cm to 1.52 cm while retaining the same overall outer dimensions. In addition, since the DC-DC converters had some thermal margin, the chassis design was modified to inhibit heat from flowing from those devices to the side walls that cooled the VME CCAs. This was accomplished with a thermal dam formed of titanium (Grade 2) interposing bars placed between the chassis bottom panel and the two side panels.

Figure 2 shows a detail view of the dam and joint. The low thermal conductivity of the titanium of 16.4 W/mK helped to reduce the flow of heat from the floor to the walls. Other environmental constraints dictated that the dams be comprised of a stiff, high-strength, lower density, electrically-conductive material. While stainless steel might have met the thermal requirements for the dam material, it added excessive weight and was not used.

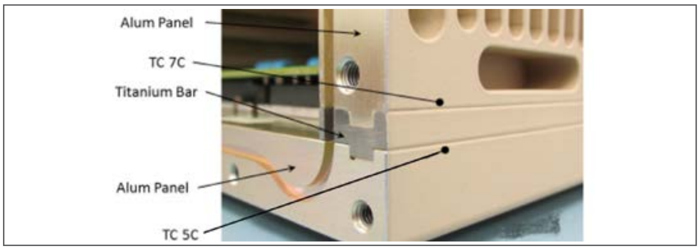

Figure 2: Chassis assembly detail showing Ti bar and aluminum panels.

A detailed thermal analysis of the custom Relay CCA was conducted to ensure that the ten microprocessor-based Solid State Relays (SSR) mounted on the board did not exceed their maximum allowable case temperature of 100°C. The FEA model initially showed that case temperature would slightly be over this limit, so the PWB design was modified to increase the number of 4 oz copper thermal planes and copper-filled vias. The effective in-plane board thermal conductivity was determined by accounting for the copper layers while the impact of the vias on the thru-plane thermal conductivity was determined using Reference [5].

A 2.0 mm via pitch was selected for the thermal via arrays as the best compromise between thermal performance, circuit routing complexity and cost for this situation. These changes reduced the maximum case temperature to ~97°C as shown in *Figure 3*.

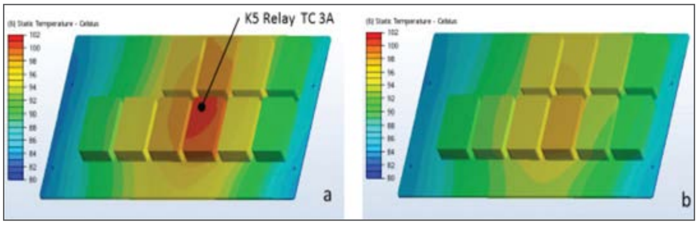

Figure 3: Thermal analysis (conduction) of relay CCA: (a) initial design, and (b) modified design with additional thermal planes and filled, thermal vias.

With these design changes implemented, along with other refinements CFD simulations of all but one of the six operational configurations (A, B and C, with and without solar loading) met requirements. The A configuration with maximum power dissipation 137 W along with the solar load did produce VME card edge temperatures that exceeded design requirements. However, the A configuration is limited to stationary ground level operation in which a solar shade can be easily employed to prevent direct solar loading, and thereby provide for satisfactory operation. *Figure 4* provides a cut-away view of the temperature results from the analysis for 137 W peak internal thermal load without the solar load.

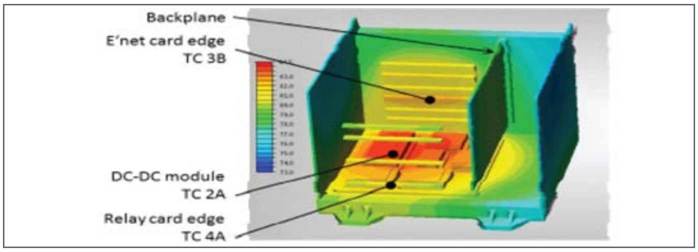

Figure 4: Temperature profile from analysis, 49°C amb., peak load, without solar lead.

TEST

A comprehensive thermal survey was conducted to verify the thermal design and validate the simulations. The unit was instrumented with twenty-four Type T thermocouples (see Figs. 2, 3, & 4 for locations; TC4B is not shown) with maximum uncertainty of 1.5°C. To more realistically test worst-case conditions, the chamber blower was turned off at 1216 minutes.

This eliminated the unrealistic convection cooling that would otherwise result from the chamber blower, so that the unit would only be cooled by natural convection and radiation. Shutting off the blower caused all the unit temperatures to increase while the chamber temperature drooped due to heat loss to the surroundings. This droop in chamber ambient is directly seen in thermocouple 8°C in *Figure 5*.

The unit temperatures stabilized ~ 3 hours after the chamber was turned off. Each temperature was averaged over a fifty-minute period from 1,400 minutes to 1,450 minutes while the average chamber ambient air temperature was 46.8°C. Average temperatures are shown in *Table 1*, which also shows ambient-corrected temperatures to reflect the chamber being 2.2°C below the 49°C requirement.

This table also shows the corresponding temperatures from the CFD analysis for the thermocouples. A comparison between the results of the test and simulation is given in that table. In general, the analysis agrees within ±5°C of the testing, which is a design objective [6].

Location 4B (the Temperature Sensor I/C mounted on the Backplane) is the only example of a test measurement more than 5°C different than predicted by CFD. This is thought to be due to the CFD model having an unrealistic space above the backplane in that location. Simulations predicted that natural convection cells with flows as high as 5 cm/s would occur in this region. In reality, the air space between VME CCAs was less than 1.5 cm, which greatly inhibited induced air flow.

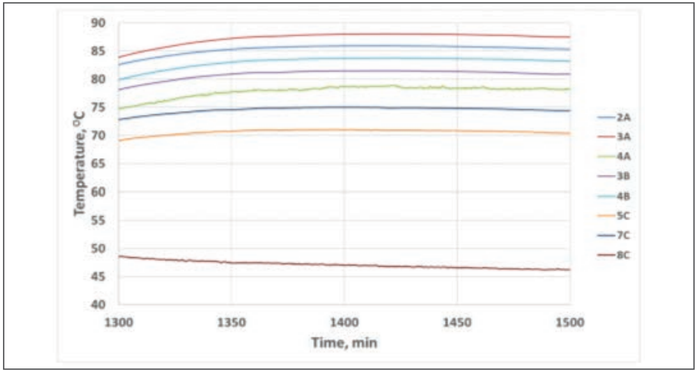

Figure 5: Thermal test results versus time for select locations. Average values were calculated for the time period 1,400 to 1,450 minutes.

The temperature difference between thermocouple 5°C (on the chassis bottom panel immediately adjacent to the titanium bar, see *Figure 2*) and location 7°C (on the chassis side panel, immediately adjacent to the titanium bar) represent the temperature drop across the bar. While CFD predicted a ΔT of 2.9°C, the test found a ΔT of 4.0°C, which indicates that the thermal dam actually was somewhat more effective than had been predicted.

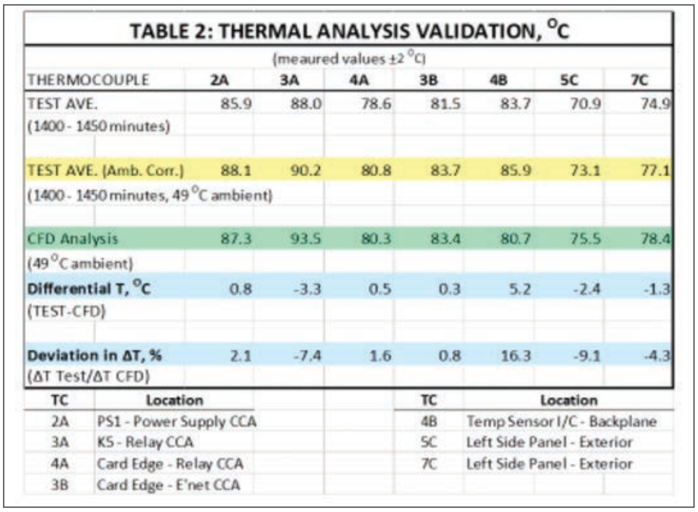

TABLE 2: THERMAL ANALYSIS VALIDATION, °C

(meaured values ±2 °C)

THERMOCOUPLE	2A	3A	4A	3B	4B	5C	7C
TEST AVE. (1400 - 1450 minutes)	85.9	88.0	78.6	81.5	83.7	70.9	74.9
TEST AVE. (Amb. Corr.) (1400 - 1450 minutes, 49 °C ambient)	88.1	90.2	80.8	83.7	85.9	73.1	77.1
CFD Analysis (49 °C ambient)	87.3	93.5	80.3	83.4	80.7	75.5	78.4
Differential T, °C (TEST-CFD)	0.8	-3.3	0.5	0.3	5.2	-2.4	-1.3
Deviation in ΔT, % (ΔT Test/ΔT CFD)	2.1	-7.4	1.6	0.8	16.3	-9.1	-4.3

TC	Location	TC	Location
2A	PS1 - Power Supply CCA	4B	Temp Sensor I/C - Backplane
3A	K5 - Relay CCA	5C	Left Side Panel - Exterior
4A	Card Edge - Relay CCA	7C	Left Side Panel - Exterior
3B	Card Edge - E'net CCA		

CONCLUSIONS

It was anticipated at the outset that there would be significant thermal management challenges to satisfactorily endure each of the environments and operating configurations required for this system. The Thermal Survey confirmed that, although the COTS CCAs and DC-DC converters operate very close to their extreme limits, the operating temperatures are acceptable. Under the most severe, worst-case conditions, the COTS CCAs card edge temperatures are within approximately 2°C of their acceptable maximum continuous operating temperature and the DC-DC converters baseplate temperatures are within approximately 12°C of their acceptable maximum continuous operating temperature. The electronics unit has successfully passed comprehensive qualification testing and has since seen actual battleground deployment.

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A Novel Approach to Development of a Thermal Capacitor

Naveenan Thiagarajan, Peter deBock, Bill Gerstler, Gary Quackenbush

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Lead research engineer at GE Global Research in Niskayuna, New York. His research includes development of novel thermal management technologies for aviation, healthcare and transportation systems. Before starting this role in 2013, he received his MS and PhD in Mechanical Engineering at Auburn University, Alabama where he focused on the development of phase change liquid cooling techniques for high power electronics in terrestrial and reduced gravity environments. Dr. Thiagarajan holds one granted patent along with more than 7 pending patents. He also has more than 10 peer-reviewed articles and publications in the field of thermal management.

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Bill Gerstler

Received his PhD in Mechanical Engineering from the University of Minnesota. Since coming to GE Global Research in 2001, he has worked in the area of thermal management including system level aviation thermal management, thermodynamic cycles, rotating electric machines, electronics, and absorption technology. He has completed system level assessments for internal programs investigating advanced commercial aircraft engine systems. He has also acted numerous times as a thermal management subject matter expert (SME) for U.S. Military programs. Bill has over 24 conference and journal publications. He also has 25 U.S. patents granted with 34 pending patents. He is a Fellow of ASHRAE.

Gary Quackenbush

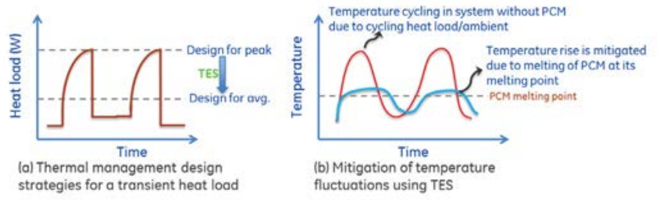
Based in Grand Rapids, Michigan and works for GE Aviation Systems, within the Chief Engineer's Office. He serves as a Chief Consulting Engineer and manages the Avionics business technology portfolio. In this role, he is responsible for the execution and selection of the internal research and development projects, links the business technologists to GE's Global Research Centers, fosters the creation of intellectual property, and engages in external technology funding pursuits. Gary has significant experience in solving our customers' problems for civil and military airborne platforms. He has worked in avionics engineering development and management and related technologies for the past 34 years.

INTRODUCTION

In terrestrial or air-borne electrical and electronic systems, cooling requirements can be unsteady due to spikes in heat load, or changes in ambient conditions. Such an event results in a sharp rise in system temperature or temperature cycling thus possibly reducing the system reliability. In the electrical domain, fluctuations in voltage are managed by using an electrical capacitor that can be charged and discharged depending on the fluctuating environment. The lack of an effective thermal capacitor in the thermal domain has often led to designs that are oversized and focused on the peak worst-case scenario. Such a design strategy leads to an increase in system size and weight, which is typically undesired, especially for an airborne system. In this article, a thermal capacitor refers to a device capable of mitigating temperature rise or fluctuations by absorbing and releasing thermal energy.

To optimize thermal designs such that they can be designed for an average heat load instead of a peak condition (*Figure 1a*), a thermal capacitor is needed. A key technique in the thermal domain that closely resembles an electrical capacitor is Thermal Energy Storage (TES). TES uses a phase change material (PCM), which upon absorption of heat from the system undergoes a solid-to-solid, solid-to-liquid, or liquid-to-gas phase transformation. Among these, solid-to-liquid phase change (melting of the PCM) is the most widely used TES system as it exhibits a lower volume expansion compared to a liquid-vapor phase change, and the latent heat of solid-to-solid phase change is typically lower than 100 kJ/kg [1] compared to latent heat of melting ranging between 200-300 kJ/kg for organic PCMs [2]. Phase change processes take place isothermally at their melting points, thus reducing the temperature rise of the systems that are thermally coupled to the PCM (*Figure 1b*).

In an aircraft, the electronic components are typically installed in designated avionics bays or equipment bays that are conditioned to maintain a temperature of approximately 55 °C. With increasing capabilities of the avionics, the heat load rejected to the environmental control system (ECS) increases. In a closely packed avionics bay the avionics chassis must have a good thermal design to prevent overheating or require excessive cooling air [3]. Additionally, avionics systems could also undergo transients in ambient temperature (potential increase up to 70 °C from steady state conditions) or loss of air cooling, arising from scenarios such as a stranded aircraft on a tarmac or an engine failure.



(a) Thermal management design strategies for a transient heat load

(b) Mitigation of temperature fluctuations using TES

Figure 1: Effect of TES on transient load thermal management

Figure 1: Effect of TES on transient load thermal management

Adequately designed TES systems could, by delaying temperature rise, play an important role in providing additional time for the reliable operation of avionics without compromising functionality. In the absence of TES systems, typical strategies involve down-clocking the computational systems to reduce temperature rise at the cost of reduced system capability.

A TES system typically consists of a hermetic enclosure which contains the PCM. One of the functions of the enclosure is to transport heat into the PCM material. An ideal thermal capacitor/TES system has an infinite energy storage capacity and a zero thermal resistance from exterior walls to the PCM material. However, in reality a TES system is rendered less effective due to the poor thermal conductivity of organic or inorganic PCM (0.2-0.5 W/m-K) and the distance over which heat is conducted from exterior to the center of PCM, depending on the form factor of the PCM enclosure. While many studies have shown that thermal conductivity of PCMs could be improved by using additives and fillers, such as graphite and carbon micro structures [4-7], to approximately 2-5 W/m-K, the thermal resistance benefit is still modest and the possible complexity of using fillers could prove prohibitive for productization.

The formulation for 1-D thermal resistance of a solid wall, based on the Fourier's law of conduction, is given in *Equation (1)*. From this equation, it can be inferred that besides increasing the thermal conductivity (kpcm), the thermal resistance could be decreased by lowering the distance (L) and/or by increasing the surface area (A) over which heat is conducted. Although thermal resistance applies only for a steady state system, the phase change process in a TES system could be considered as a quasi-steady state process.

$$R_{cond} = \frac{L}{k_{PCM}A} = \frac{T_h - T_{PCM}}{Q} \tag{1}$$

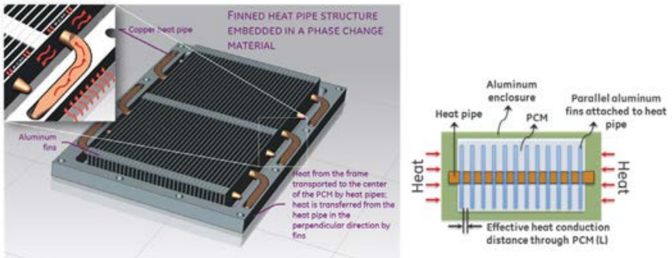
Where L = Length of heat conduction through the PCM (m)
A = Surface area (m2)
k_{pcm} = Thermal conductivity of PCM (W/m-K)
R_{cond} = Conduction thermal resistance through the PCM (°C/W)
T_h = Temperature of heated surface (°C)
T_{PCM} = Temperature of PCM (°C)

This article focuses on the development of a modular, scalable TES enclosure with a low thermal resistance (0.1 °C/W) achieved by minimizing the ratio of L/A .

DEVELOPMENT OF A 3U THERMAL ENERGY STORAGE CARD

The aforementioned design principle of minimizing "L/A" was used in the development of a prototype 3U (a standard form factor of an electronic card) TES card for use in a Line Replaceable Unit (LRU) avionics chassis. An LRU chassis has a number of slots in which electronics cards can be installed. If the chassis slots are not completely filled, one or more TES cards can be added in the available slots to increase the thermal capacitance of the system. Although this version focused on development of a TES system for avionics, the designed thermal capacitor, reported in this study, has broad applicability for any application that has a varying duty cycle (i.e. high peak loads or boundary conditions that limit the design).

A device that closely resembles the required combination of high surface area and small conduction distance is a parallel plate electrical capacitor where the electrical capacitance is directly proportional to the surface area and inversely proportional to plate spacing. Analogous to a parallel plate capacitor, a structure was developed that consists of a parallel network of heat pipes that extend from the walls of the TES enclosure at one end, and attached to tightly spaced parallel plate fins embedded in the PCM at the other end.



(a) Heat transfer in a finned heat pipe structure embedded in PCM (not drawn to scale) [8]

(b) Assembly of TES enclosure with finned heat pipe structure

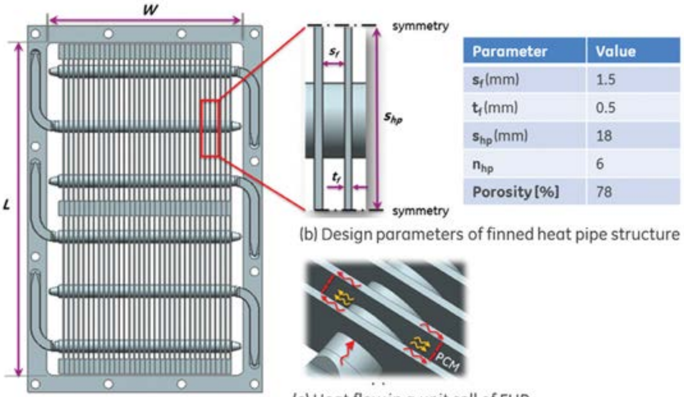
Figure 2: Schematic representation of a thermal capacitor with a finned heat pipe structure

These heat pipes form the primary low thermal resistance conduction path from the walls to the center from where heat is distributed laterally in the aluminum fins as shown in *Figure 2*. Such a structure results in a congruent isothermal melting process over the volume of the enclosure while maximizing the surface area and porosity for heat transfer and storage, respectively. A schematic layout of the finned heat pipe structure (FHP) to explain the nomenclature involved in the design is shown in *Figure 3*.

An attractive feature of the finned heat pipe structure (FHP) developed is the adaptability and scalability to other applications owing to its simple architecture. For a given application with its energy storage or temperature stability requirements, the design of FHP structure involves optimization of the key parameters listed below to achieve a target thermal resistance:

- number of heat pipes (nhp)
- spacing between heat pipe (shp)
- number of fins (nf)
- fin spacing (sf)
- PCM material melt temparture (Tmelt,pcm)

The structure shown in *Figure 3* was optimized to result in a thermal resistance < 0.1 °C/W (defined as shown in *Equation 1*) measured at the end of phase change, from exterior side wall to PCM center. Optimization of the FHP structure for the target application will be part of a separate study and hence not reported in this article. The optimized parameters are shown in *Figure 3b*. The resulting porosity (volume available for PCM in the enclosure) of the optimized finned heat pipe structure is 78%. This is comparable to the porosity of foam structures which could be up to 90-95% [9].



Parameter	Value
s_f (mm)	1.5
t_f (mm)	0.5
s_{hp} (mm)	18
n_{hp}	6
Porosity [%]	78

(a) Plan view of finned heat pipe structure

(b) Design parameters of finned heat pipe structure

(c) Heat flow in a unit cell of FHP

Figure 3: Nomenclature of a finned heat pipe structure

For a PCM enclosed within tightly spaced fins, convection effects of melted PCM are negligible as the buoyancy forces in such thin spaces are not sufficient to overcome the viscous forces. This can be expressed non-dimensionally using Rayleigh number (Ra). The critical Rayleigh number (Racr) over which buoyancy dominates is 1708 [10]. In comparison, the fin spacing of 1.6 mm results in a Ra lower than 1708, indicating that the dominant mode of heat transfer is conduction. This allows for a simpler 1-D/2-D conduction model to be used in the design of finned heat pipe structure depicted in this study.

It should be noted that the benefit of a thermal enhancement structure, such as a finned heat pipe, is reduced in a thin spread-out PCM volume placed on a thermally conductive surface owing to the small conduction lengths in the direction of heat transfer. In the current study, with heat application at the sides, the effective conduction length without any embedded structure is one-half of the width of enclosure, which is 42 mm. With the addition of finned heat pipe structure the effective conduction length has been reduced to 0.8 mm, which is one-half of the fin spacing (52.5x improvement).

EXPERIMENTAL EVALUATION OF THE FINNED HEAT PIPE STRUCTURE

A prototype 3U TES card with the aforementioned FHP parameters was developed for experimental performance validation. An experiment was devised to quantify the benefit of the FHP structure. A test system was developed to add heat to the system at the side-rails (similar to an LRU chassis) while measuring temperature of the heaters and PCM during the process of heating.

To evaluate the effect of the finned heat pipe structure versus a system that is just filled with plain PCM, a TES enclosure without the finned heat pipe structure was also constructed as baseline. In all experiments, applied heat input was varied between 15 to 45 W and the transient temperature response of the system was recorded. Results reported in this article are limited to melting of the PCM and results corresponding to PCM re-solidification will be reported in a separate study.

Transient temperature profiles of the PCM and heated enclosure sides with and without the FHP structure heated at 30W are shown in *Figure 4*. In the absence of the finned heat pipe structure, i.e. baseline, the temperature of the heater continued to rise even after the PCM started melting at 69 °C (red dotted line). It was also noticed that the difference in temperature between the heated sides and the PCM center (blue dotted line) was more than 10 °C at the completion of melting. This is mainly due to the aforementioned high thermal resistance of the phase change material arising from the poor thermal conductivity and the longer distance of heat transport (42 mm).

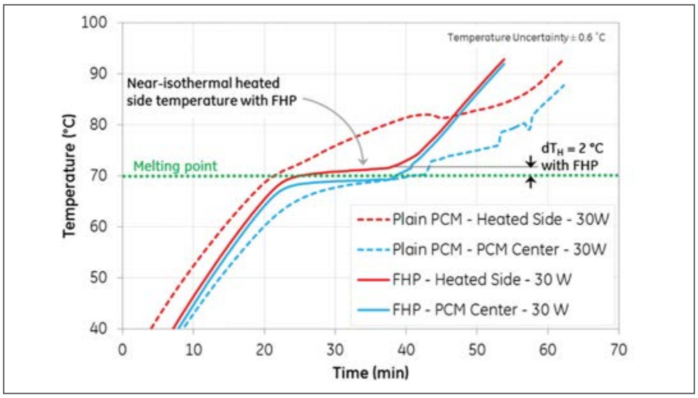


Figure 4: Comparison of heater and PCM temperatures between plain PCM and thermal capacitor consisting of finned heat pipes at 30 W

In the case where the finned heat pipe structure was employed, once the melting point of PCM was reached, the heater temperature (red solid line) was observed to be near-isothermal and the observed temperature difference between the heated sides and the PCM at the center (blue solid line) was less than 2 °C. This result is attributed to the significant lower thermal resistance resulting from the lower conduction distance through the PCM between the fins (0.8 mm).

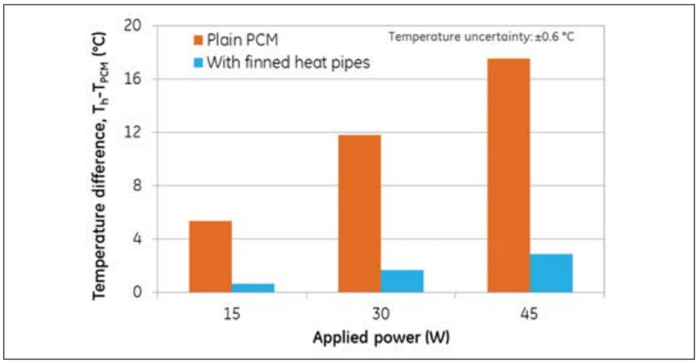


Figure 5: Measured temperature difference between the heater and PCM at the completion of phase change with and without FHP structure

In *Figure 5*, the effect of applied power on the reduction in temperature difference between the heater and PCM center due to FHP is illustrated. At 45 W, the temperature rise of heater above the melting point of PCM is 3 °C with FHP and 18 °C without the FHP, further demonstrating the improved near-isothermal phase change performance of the prototype at all tested conditions compared to the baseline. The low thermal resistance of the designed architecture not only aids in faster charging of PCM, but also faster discharging of heat, thus enabling the use of the designed TES system for higher frequency of transient heat pulses.

FIGURE OF MERIT AND COMPARISON WITH LITERATURE

An ideal TES system possesses an infinite energy storage capacity and a low thermal resistance (low temperature rise of the heated system) which enables rapid charging and discharging. Based on these characteristics, an effective heat capacitance (Ceff) during phase change is defined, as shown in *Equation (2)*, which has to be maximized for a TES system to be effective

$$C_{eff} = \frac{Q \times dt}{(m.dT)_H + (m.dT)_{PCM}} \tag{2}$$

where C_{eff} = System thermal capacitance (kJ/kg-K))
Q = Heat supplied (W)
dt = Time between start and end of melting process (s)
m = Mass (kg)
dT = Temperature difference between completion and beginning of PCM melting process (°C); subscript 'H' and 'PCM' represent the temperature rise of heater and PCM during the phase change respectively

To illustrate the importance of the surface area to volume ratio, known as the specific surface area (β), *Equation 2* can be re-arranged to give:

$$C_{eff} = \frac{q" \times \beta \times dt}{\{\rho(1-\varepsilon).dT\}_{Al} + \{\rho\varepsilon.dT\}_{PCM}} \tag{3}$$

where q" = Heat flux (W/m^2)
V_{tot} = Total volume (m^3)
ε = Porosity (-)
β = Specific surface area = A_s/V_{tot} (m^{-1})

It can be inferred that increasing the surface area to volume area ratio will increase the effective thermal capacitance or the storage capacity. In the current design of FHP, the specific surface area is approximately 910 m-1 which is comparable to finned structures and matrices used in many compact heat exchangers [11].

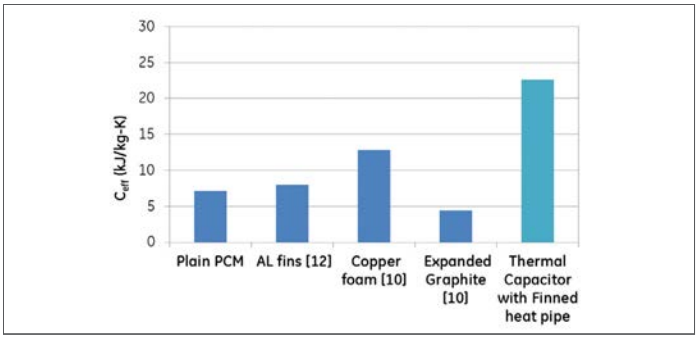


Figure 6: Comparison of effective thermal capacitance with other thermal enhancement structures found in literature

Figure 6 represents the effective specific heat of the thermal energy storage system compared against other techniques used to improve the thermal resistance of PCM. The higher capacitance of the finned heat pipe structure is directly a result of the low temperature rise of the heater over the melting point (2 °C at 30 W). It must be noted that comparison with literature was only made with systems that do not have a thin form factor in the direction of heat transfer as the role of thermal enhancement structure in thin PCM volumes are limited owing to the inherent small conduction lengths.

CONCLUSION

An effective thermal capacitor is developed that minimizes conduction length through the PCM by more than 50 times and maximizes surface area by the use of a finned heat pipe structure embedded in the PCM. The structure can be engineered to yield desired temperature rise and porosity specifications for most applications with conventional manufacturing techniques. A unique aspect of the thermal capacitor design is that it is modular such that it can be scaled up to larger volumes, yet still providing a low thermal resistance from walls to PCM. The concept of such thermal capacitor was demonstrated by evaluating the performance of a 3U thermal energy storage card for an LRU avionics system.

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Delphi4LED - From Measurements to Standardized Multi-Domain Compact Models of Light Emitting Diodes (LED)

Genevieve Martin*, Andras Poppe, Sangye Lungten, Veli Heikkinen, Joan Yu, Marta Rencz, Robin Bornoff
*Corresponding Author

INTRODUCTION

The rise of LED technology is changing the ecosystem of the lighting industry. Delphi4LED [1] is a European Union consortium that is responding to these changes by providing the EU LED Lighting industry with a set of tools and standards to enable the design and production of more reliable, cost effective and market-leading LED-based lighting solutions.

Currently, LED datasheets report a single figure of merit: the thermal resistance, Rth. This figure of merit is generally specified for one ill-defined operating condition and does not adequately address the intertwined relations among optical, thermal, and electrical performance requirements. Effective luminaire design requires more granularity than is currently available in conventional LED datasheets. A comprehensive mathematical description of LEDs that includes thermal, optical, and electrical performance is needed to establish the complete working space of each LED used at luminaire levels. This will allow designers to account for the effects of other LEDs and electronic components.

THE DELPHI4LED MISSION

The adoption of Light Emitting Diode (LED) shifts the lighting industry's market and supply chain boundaries from those established by the conventional lighting industry. What was essentially an oligopolistic industry that has been dominated by European companies is rapidly becoming a more competitive environment that includes worldwide players from industries other than LEDs, such as sensors & controls and integrated circuit technologies.

The conventional lighting market, which has traditionally been significantly driven primarily by replacement needs, is substantially being altered by the growing use of LEDs. With the longer life of LEDs, the replacement market is seeing a natural decline as consumers need to replace their light source less often. This is projected to cause the total light source market to flatten out after 2016 [2]. This in turn will accelerate the value shift from light sources towards fixtures as well as lighting system controls. This emerging new arena impacts the distribution channel structure of the market environment. The importance of technical know-how is increasing, particularly in professional distribution channels, due to LED and lighting controls system penetration.

The Delphi4LED consortium provides a holistic response to this market transition by combining the competitive lighting knowledge base in Europe with new paradigms and corresponding solutions

Genevieve Martin

Genevieve Martin is the project coordinator of Delphi4LED. As a Principal Engineer and Competence Leader of Thermal Management and Mechanics, she is responsible for driving the roadmaps and research program of the thermal and mechanics competence areas for global Philips Lighting. She holds a master degree from Université de Technologie de Compiègne (F) and an MBA from TiasNimbas Tilburg (NL). Genevieve joined Philips in 1998, after having worked four years at CERN. She has broad experience in the thermal management of systems in lighting and healthcare. She used IC compact thermal models as a thermal engineer for television products and began working on LED products in 2007 as part of Philips Research before joining Philips Lighting in 2014.

In addition to her activities at Philips, she is member of the technical committee and program committee of the SEMI-THERM conference and was the general chair of SEMI-THERM 30 in 2014.

to the product creation process. The primary goal is to simplify the early development phase by standardizing Compact LED models for design and simulation. Standardized Compact Models of LEDs, which do not yet exist, will be implemented with models of other electronic and mechanical components to establish a more unified computer-based design and simulation environment for integrated lighting products.

Introducing standard data interfaces, design methodologies and tools will bridge the design gaps between different players and disciplines in the Solid State Lighting (SSL) ecosystem by:

- accelerating the development, and improving the accuracy, of product performance predictions while minimizing the need for building physical prototypes,
- reducing the price point of the resulting solutions,
- increasing options for introducing greater creativity in systems and solutions.

ADDRESSING THE TECHNICAL CHALLENGES

The main challenge for designing LED components into lighting systems is determining the correct LED inputs. Currently, input is provided in the form of a single figure of merit: the thermal resistance, Rth. This figure of merit is generally specified for one ill-defined operating condition and does not adequately address the intertwined relations among optical, thermal, and electrical performance requirements. This lack of information is due to the ill-defined characterization of LEDs, which is exacerbated by the need for LED suppliers to protect their intellectual property.

Figure 1 illustrates the need to have a comprehensive mathematical description of LEDs that includes thermal, optical, and electrical performance to establish the complete working space of each LED used at luminaire levels. This will allow designers to account for the effects of other LEDs and electronic components.

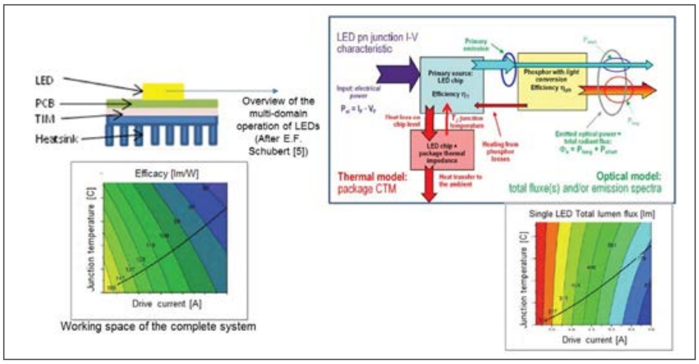


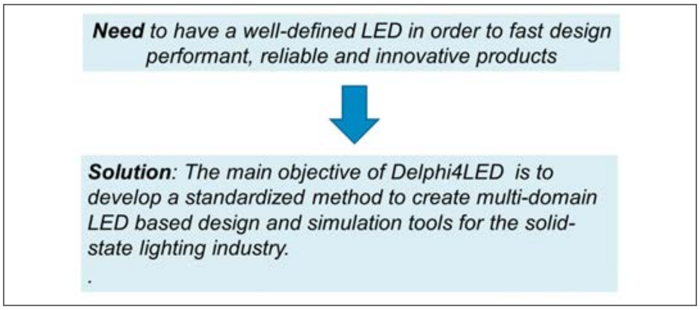
Figure 1 - Multi-domain operation of LEDs and the scope of Delphi4LED [3]

The approach proposed by Delphi4LED is to model the multi-domain nature of the LED chip such that it can be used at module and system levels [4]. When an accurate thermal model of the LED package is used with boundary conditions conforming to the actual LED use environment, temperatures can accurately be predicted at all levels within the supply chain.

MOVING TOWARDS GREATER STANDARDISATION

The design of LED systems will be significantly improved with the use of a modular, multi-domain based modelling approach. This modular approach will provide design flexibility for LED component integrators in any kind of luminaire design. Establishing this capability requires seamless integration of the LED into the product development chain.

Standardization creates a communication bridge between the semiconductor industry (LED supplier) and the Lighting industry (LED component integrators) and improves the quality of lighting design implementation. The main objective is to establish a standardized method to create multi-domain LED based design and simulation tools for the industry (*Figure 2*).



***Need** to have a well-defined LED in order to fast design performant, reliable and innovative products*

***Solution**: The main objective of Delphi4LED is to develop a standardized method to create multi-domain LED based design and simulation tools for the solid-state lighting industry.*

Figure 2 - Delphi4LED goal

To achieve this, the following tools have to be provided:

- Generic, multi-domain model of LED chips
- Compact thermal model of the LED chips' environment, including package and substrate
- Interfaces of compact models linking them with the luminaire system design

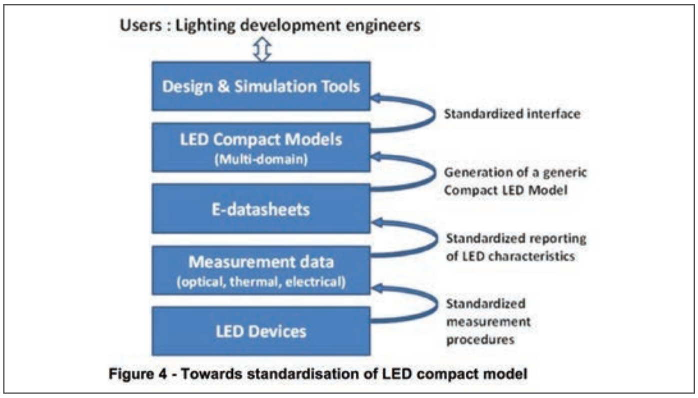


Figure 4 - Towards standardisation of LED compact model

The goal of the project is to develop a standardized method to create multi-domain LED compact models from test data (*Figure 3*).

The key objectives are to:

- Define a set of LED model equations that can be implemented into a FEM/CFD tool, for the purpose of self-consistent multi-domain simulation of an LED's thermal, electrical and light output characteristics.

- Provide interfaces between measurement tools, modeling tools and simulation tools to allow compact LED models to be applied.
- Demonstrate the benefits of using compact models in the development process to reduce development times and cost, as well as to prepare for the digital revolution (e.g. Industry 4.0).

WHO IS BEHIND THE PROJECT?

A multi-disciplinary approach has been selected by Delphi4LED to foster the adoption of its recommendations by the marketplace. At most SSL companies, thermal, optical and electrical measurements are typically treated in an isolated manner because different testing teams and labs have not been adapted to the changing landscape of the solid-state lighting industry. Although a combined thermal and radiometric/photometric testing method does exist for LEDs, it is still primarily used only in the traditional manner by LED thermal testing teams.

Due to the lack of appropriate standardized multi-domain testing protocols, these methods are not widespread in either the lighting community or among the LED suppliers. Measurement-based characterizations are completed with computer simulations.

The methodology that will be developed by Delphi4LED will be completed by end-user validation at luminaire level. The adopted methodology will not require any sharing of proprietary information from LED manufacturers. *Table 1* lists specific technical disciplines, as well as general knowledge areas, that are needed for developing successful LED lighting products.

Table - 1 LED Technical Disciplines and Areas

Disciplines	Knowledge Area
1.Laboratory testing 2.In-line testing 3.Simulations 4.Statistical analysis and mathematics 5.Data reporting 6.Computer simulation and engineering	Optical Electrical Thermal metrology Lighting systems

The Delphi4LED consortium includes 15 partners from 7 countries and brings together luminaire manufacturers, academia, and software vendors. These three areas provide the following capabilities:

- Industry partners who are involved in the direct LED value chain can provide knowledge related to the LED portfolio combined with the end-use applications.
- Academic partners can provide profound knowledge on compact model methodology, measurement techniques and model extraction for LEDs and electronic components in general.
- Software partners who develop the necessary analysis tools will provide knowledge of simulation and integration of multi-domain compact models.

The goal of the consortium is to develop methods that are component-agnostic so that the standardized model is independent from specific LED component designs. Therefore, no LED manufacturers are included in the Delphi4LED consortium to ensure that the standardization methods do not require input from an LED manufacturer.

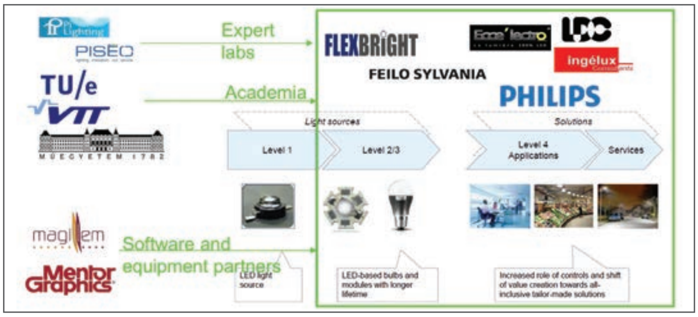


Figure 5 - The position of the consortium members in the value chain

EXPECTED IMPACT OF DELPHI4LED

The European lighting industry faces two key challenges as a result of the introduction of LED:

- On the market side, it is necessary to reduce development time, improve the quality of current LED products and emphasize value-added activities to gain competitive advantage.
- On the development side, LED lighting has challenges that differ from conventional lighting applications. New characterization procedures, as well as new standardization methods, need to be defined to accelerate the adoption of LED. This will require advances to industry standards in the lighting industry.

This project aims to reduce the time to market of LED products by one-third, cut development costs by 50%, and reduce the indirect costs related to yield by 25%. The goal is to provide the European lighting industry a unique competitive advantage to keep up with the current 30-40% rate of LED market growth and tap into potential new markets.

SUMMARY

The Delphi4LED project, which formally began in June 2016, is intended to provide an answer to rapid market transition. This project will combine the competitive lighting knowledge base in Europe with new paradigms and corresponding solutions in the product design process by developing standardized compact LED models for design and simulation.

Combining these models with models of other electronic and mechanical components will unify the computer- based design environment for integrated lighting products. Bridging the design gaps between different players in the chain will accelerate development, increase the accuracy of predictions for final products, reduce the price of LED solutions, and increase design flexibility by allowing for greater creativity freedom in systems and end-user products.

ACKNOWLEDGEMENTS

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Ingelux, France; Department of Electron Devices-Budapest University of Technology and Economics, Hungary; Mentor Graphics, Hungary

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KEYNOTE Tuesday March 14, 2017

Ultimately Dense and Efficient Future Computers

Liquid cooling enables an unprecedented density in future computers to a level similar to a human brain. This is mediated by a dense 3D architecture for interconnects, fluid cooling, and power delivery of energetic chemical compounds transported in the same fluid. Vertical integration improves memory proximity and electrochemical power delivery creating valuable space for communication. This strongly improves large system efficiency thereby allowing computers to grow beyond exa-scale. A dense and efficient µServer has been demonstrated as a first milestone along this roadmap. A universal concept is presented showing that volumetric density drives efficiency in information processing irrespective of switch technology and architecture, and can replace the currently slowing Moore's law. By adopting some of the characteristics of the human brain, computers have the potential to become far more compact, efficient, and powerful. And this, in turn, will allow us to take full advantage of cognitive computing – providing our real brains with new sources of support, stimulus, and inspiration.

Bruno Michel received a Ph.D. degree in biochemistry/biophysics from the University of Zurich subsequently joined IBM Research to work on scanning probe microscopy and later on the development of accurate large-area soft lithography. Dr. Michel started the Advanced Micro Integration group to improve thermal interfaces and minaturized convective cooling for processors and concentrated photovoltaic systems. Main current research topics of the Zurich group are microtechnology/microfluidics for nature-inspired minaturized tree-like hierarchical supply networks, 3D packaging, and thermophysics for improved understanding of heat transfer in nanomaterials and structures. Dr. Michel started the energy aware computing initiative at IBM and triggered the Aquasar project to promote improved efficiency and energy re-use in future green datacenters and photovoltaic thermal solar concentrators.

DATA CENTER KEYNOTE Wednesday, March 15, 2017

A Holistic View of a Fragmented Data Center Industry

SEMI-THERM and AFCOM are excited to have Dr. Sammakia provide the Keynote speech for the Data Center Track at SEMI-THERM 33. Dr. Sammakia's experience spans the full physical scale of IT systems (chip to chiller) and the evolution of the data center from mainframe rooms to today's distributed and cloud computing facilities. Please join us for Dr. Sammakia's unique perspective on how data centers and IT systems have evolved over the decades, the impact of this history on engineering practices and computing performance (with a focus on the Gap between IT and facilities) and where the industry is likely to head into the future.

Dr. Bahgat Sammakia is a Distinguished SUNY Professor and the vice president for research at Binghamton University. Dr. Sammakia has spent much of his research career working to improve thermal management strategies in electronic systems at multiple scales ranging from devices to entire Data Centers. Dr. Sammakia joined the faculty of the Watson School for Engineering and Applied Science in 1998 following a fourteen-year career at IBM where he worked in the area of research and development of organic electronic systems. He has contributed to several books on natural convection heat transfer and is also the principal investigator or co-principal investigator on several cross-disciplinary research projects. Dr. Sammakia received his PhD degree in mechanical engineering from the State University of New York at Buffalo. He was a post doctoral fellow at the University of Pennsylvania from 82 to 84. Dr. Sammakia is a Fellow of the IEEE, the ASME and of the National Academy of Inventors. Dr. Sammakia has over 250 publications in refereed Journals and conference proceedings as well as several books and book chapters related to electronic systems thermal management.

Luncheon Speaker Tuesday, March 14, 2017

Multi-Scale Optimization Strategies for Electronics Thermal Management & Energy Harvesting
Ercan M. Dede

The compact and power-dense nature of advanced electronics is expected to push the limits of traditional thermal management techniques. At the same time, low-grade waste heat represents a tangible source of inefficiency for future electrified systems. Exploiting effective design optimization strategies in the research and development of new cooling and material technologies enables opportunities for increased system performance. Accordingly, gradient-based structural optimization methodologies and their implementation at multiple scales is the focus of this talk. Specifically, electronics thermal management and waste heat recovery are explored as end applications. At the component level, several case studies are presented to illustrate the technical approach for air, single-phase liquid, and two-phase cooling of automotive power electronics. At the material level, thermal composite printed circuit board design for informed heat flow control and energy harvesting is outlined. Through these various examples, multi-scale optimization is revealed to be an essential element in the drive towards novel high performance thermal energy management technologies.

Ercan M. Dede received his B.S. degree and Ph.D. in mechanical engineering from the University of Michigan and an M.S. degree in mechanical engineering from Stanford University. Currently, he is a manager in the Electronics Research Department at the Toyota Research Institute of North America. His group conducts research on advanced vehicle electronics systems including power semiconductors, advanced circuits, packaging, and thermal management technology. He has over 30 issued patents and has published more than 40 articles in archival journals and conference proceedings on topics related to design and structural optimization of thermal, mechanical, and electromagnetic systems.

Luncheon Speaker Wednesday, March 15, 2017

Reducing Earthquake Hazards at Manufacturing Facilities
Guna Selvaduray, Ph.D.

Since the Loma Prieta Earthquake of October 17, 1989 the San Francisco Bay Area has not experienced a major earthquake. This presentation will begin with a brief description of the earthquake threat faced by the urbanized SF Bay Area, with a focus on the fault lines that run through this region. The major part of this presentation will focus on the damage that the industries in the Kansai Region in Japan experienced during the Kobe Earthquake of Jan 17, 1995, and the lessons that were learned from that unfortunate experience. Examples (slides) of damage to buildings and equipment, a summary of the research findings intended to reduce damage and accelerate recovery, and mitigation measures that can be taken ahead of time to reduce damage, especially for production and laboratory equipment will constitute a major part of this presentation.

Dr. Guna Selvaduray earned his M.S. and Ph.D. degrees from Stanford University and his B. Eng. degree from Tokyo Institute of Technology. His research has focused on nonstructural hazard mitigation, hazardous materials problems caused by earthquakes, and protection of building contents and plant equipment from earthquake damage. He has been the recipient of research grants from the National Science Foundation, the Department of the Interior and the California State Government. At San Jose State University, Dr. Selvaduray created the Collaborative for Disaster Mitigation (CDM), a public-private-academic partnership that has focused on implementing hazard mitigation in order to achieve loss reduction.

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A History of Commercial CFD from Bernoulli to Spalding and Beyond, with a Focus on Electronics Cooling Simulation

Robin Bornoff, Mentor Graphics **John Parry, Mentor Graphics**

Since the early 1980s, commercially available CFD tools have evolved to play a central role in engineering design today. Limited by available compute power, CFD technologies were devised that offered usefully accurate results but required a high level of fluid dynamics and programming skills. The last 3 decades have seen a revolution in the industrial adoption of commercial CFD and widespread adoption for electronics cooling, due to compute power limits being relaxed, novel techniques developed, and usability enhanced. This short course tracks the rise of commercial CFD, in terms of technological capability, the impact of an ever-evolving hardware compute roadmap, integration into a wider design environment, and changing user persona. We will review the lessons learnt during this period, from compact modelling of complex and IP-restricted electronic parts, to pragmatic approaches that bring the power of simulation to bear on the initial architectural phase of product design. Illustrative examples will show how CFD has impacted different aspects of thermal design across packaging levels and stages in the development process.

Robin Bornoff attained a Mechanical Engineering Degree from Brunel University in 1992 followed by a PhD in 1995 for CFD research. He then joined Mentor Graphics Corporation, Mechanical Analysis Division (formerly Flomerics Ltd) as an application and support engineer, specializing in the application of CFD to electronics cooling and the design of the built environment. He is now Market Development Manager for the Physical Design of Electronics in the Mechanical Analysis Division.

John Parry attained a Chemical Engineering Degree from Leeds University in 1982, and a PhD in 1988. He joined Mentor Graphics Corporation's Mechanical Analysis Division in 1989 to manage its customer services operation, and later head its research activities. John has coordinated several collaborative research and knowledge transfer projects. With over 75 published technical articles, he is a member of JC15 and past chair of SEMI-THERM and has 4 patents pending.

Short Course 2 **Morning** **Monday, March 13, 2017**

Fundamentals of Liquid Cooling: From Fluid Selection to Phase Change

Timothy Shedd, Ebullient Inc.

This short course will provide attendees with the tools they need to design liquid-cooled thermal management systems for virtually any challenge they may face. The course will begin with a review of the engineering fundamentals that form the basis for design and prediction of convective heat transfer on simple and complex surfaces. Next, we will apply these fundamentals to develop an objective, thermodynamic criterion for comparing arbitrary fluids on their merits. Proceeding to single-phase flows, we will compare the tradeoffs of different surface enhancements as well as employing more advanced techniques, including spray and jet impingement. We will look at practical examples of natural convection and how to estimate the performance of immersion cooling, which can be quite effective without active pumps. The final section of the course will cover an introduction to boiling and how to employ phase change in electronics cooling. Every topic in the course will be accompanied by practical examples and solutions methods that can be implemented, where possible, in common spreadsheet software.

Dr. Timothy Shedd had an early passion for technology and sustainable energy which led him to obtain a B.S. in Electrical Engineering from Purdue University in 1992. He began working with the Semiconductor Engineering Group at Digital Equipment Corporation (now part of Intel), and was a designer of the world's fastest commercial CPUs from 1988 through 1995. At DEC, Dr. Shedd first learned how computing power was limited by heat produced at the chips, and he helped to design one of the first commercial CPUs with active power control. Dr. Shedd completed M.S. and Ph.D. degrees in Mechanical Engineering from the University of Illinois at Urbana-Champaign. He became a professor of Mechanical Engineering at the University of Wisconsin-Madison in 2001, publishing over 45 peer-reviewed journal articles and many more conference and symposia publications. Dr. Shedd founded Ebullient in 2012. He is now full time with Ebullient as its CEO and CTO.

Short Course 3 **Morning** **Monday, March 13, 2017**

Transient Thermal Analysis Using Linear Superposition

Roger Stout, ON Semiconductor

The mathematical principle of linear superposition is a powerful and useful method of analyzing many thermal problems. This course will show how it may be applied to semiconductor and more general electronics packaging and system situations, in particular for time-varying power inputs to single and multiple heat-source applications. The "method of images" will be demonstrated for creating transient simulations of certain classes of non-symmetric thermal problems from simpler solutions. The use and significance and implications of Foster and Cauer thermal RC networks for transient analysis will be covered. Various features of Microsoft Excel as a tool for performing thermal analysis will be presented, including the use of Visual Basic. Multiple heat-source steady-state thermal problems, are, of course, a special case of transient analysis and will also be considered. Limitations of linear superposition will be discussed.

Roger Stout received his BSE in Mechanical Engineering at ASU in 1977, and as a Hughes Fellow earned his MSME at the California Institute of Technology in 1979. His full-time career then began at Motorola, which in 1999 launched its first spin-off, ON Semiconductor, where today Roger manages the Thermal and Mechanical Characterization Lab, which is part of the Packaging Technology Development organization within ON's Corporate Research and Development division in Phoenix, AZ. Roger has authored and coauthored more than 70 technical papers and presentations. He has been a peer reviewer for the IEEE TCPT Journal (and others). Roger holds six patents, and has been a registered Professional Engineer (Mechanical) in the state of Arizona since 1983.

Short Course 4 **Afternoon** **Monday, March 13, 2017**

Spreadsheet Based Thermal Analysis Method

Ross Wilcoxon, Rockwell Collins

This course will show the attendees methods for using spreadsheets to do a variety of typical thermal analyses. It will begin with a brief overview of spreadsheet functions on cells and arrays as well as methods for more easily controlling the input and output of spreadsheet tools. This will be followed by discussions on the analysis of situations such as a thermal resistance network, flow within a chassis, uncertainty analysis of a thermal test stand and transient thermal behavior. Students will be provided with example spreadsheets that can be adapted for their own analysis needs.

Ross Wilcoxon is a Principal Mechanical Engineer in the Rockwell Collins Advanced Technology Center. He conducts research and supports product development related to component reliability, electronics packaging and thermal management. He has contributed to the development of multiple systems for communication, processing, displays and radars for commercial and military avionics applications. His research areas have included rapid test methods for evaluating component reliability, heat pipes, liquid metal cooling, advanced composites and tin whisker mitigation. He is a past chair of the SEMI-THERM conference, has dozens of conference and journal publications and holds 29 US patents. Prior to joining Rockwell Collins in 1998, he was an assistant professor at South Dakota State University. He received B.S. and M.S. degrees in mechanical engineering from South Dakota State University and a Ph.D. in mechanical engineering from the University of Minnesota.

Short Course 5 **Afternoon** **Monday, March 13, 2017**

Design of Experiments for Thermal Engineering

James Petroski, Design By Analysis

This course is intended to introduce people to the concept of Design of Experiments (DOE) and how it can be applied to engineering for effective design and experimentation. Beginning with a discussion of effective experimentation, the class will progress through different types of experimentation used today, the role of statistics in planning experiments and the product designs they influence, to an overview of various types of DOE's. In depth presentation of certain DOE types will be given and the reason why the DOE type is chosen for a particular situation. The course will then show the process of setting up a "typical" DOE and follow with two examples, one from an analytical design using a DOE and a second of an experimental DOE of a system.

James Petroski is the founder and Principal Consultant of Design by Analysis Technical Consulting. Mr. Petroski has been involved in thermal, shock and vibration management of electronics systems for DOD, NASA and commercial applications with over 35 years' experience in the field of electronics packaging and LED thermal management. He received his Bachelor's in Engineering Science and Mechanics from Georgia Tech and a MS degree in Engineering Mechanics from Cleveland State University. He has authored numerous papers related to LED and electronics packaging, has thirty patents pertaining to solid-state lighting, and is currently a member of the ASME K-16 Subcommittee on Heat Transfer in Electronics.

Short Course 6 **Afternoon** **Monday, March 13, 2017**

Fundamentals of Power in the Data Center
Brian Zahnstecher, PowerRox

Power electronics in data center hardware can make or break the ability to enable an implementation for success or not. A common industry practice is to use simplified assumptions for loading and power conversion efficiency to provide approximate calculations of power utilization. Unfortunately, implementers find huge errors and variability between predicted and actual power consumption, which yield very costly (in CAPEX, OPEX, and time) headaches for many stakeholders. This is due to oversimplification of the highly convoluted and transient nature of power loading in the data center.

This entry- to intermediate-level Short Course will provide an in-depth investigation into what drives power requirements in data center equipment. The first part will focus on key attributes of data center hardware system power budgets. The second part will focus on rolling-up what was learned about power budgets at the system-level into the rack, aisle, and complete data center levels to provide the full picture of the data center power solution all the way from the load to the building inputs.

Brian Zahnstecher is a Sr. Member of the IEEE, Chair of the IEEE SF Bay Area Power Electronics Society (PELS), and the Principal of PowerRox, where he focuses on power design, integration, system applications, and OEM market penetration, and private seminars for power electronics. He previously held positions in power electronics with industry leaders Emerson Network Power, Cisco, and Hewlett-Packard, where he advised on best practices, oversaw product development, managed international teams, created/enhanced optimal workflows and test procedures, and designed and optimized voltage regulators. He holds Master of Engineering and Bachelor of Science degrees from Worcester Polytechnic Institute.

How-To Courses **Wednesday Evening March 15, 2017**

Practical Guidelines for Using Heat Pipes and Vapor Chambers in Heat Sinks	Presenter: George Meyer
Thermocouple Theory and Practice	Presenter: Bob Moffatt
Design of Liquid Cooled Systems	Presenter: Pablo Hidalgo, Thermacore, Inc.
Design Consideration for Heat Sink Mounting Solution	Presenters: Dr. Milena Vujosevic, Intel Juan L. Cruz, Light

VENDOR WORKSHOPS Afternoons Tuesday March 14 and Wednesday March 15

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Tuesday Evening Presentation **A Decade of Data Center Efficiency: What's Past is Prologue!**

Presenter: Jonathan G. Koomey, PHD

In 2006, EPA's ENERGY STAR group brought the information technology industry together twice to discuss energy efficiency in data centers. Electricity use of these facilities had doubled in the preceding 5 years, and most folks in the industry knew something had to be done.

Since then, server manufacturers have redesigned their devices to reduce power use when idle, highly efficient data center modules have become commonplace, virtualization of workloads is routine, efficiency metrics are in widespread use, cloud computing is a well known term, and the most sophisticated owner operators use engineering simulation to better manage design and operation of their facilities.

The results have been dramatic. Total electricity used by data centers in the US has grown little since 2007, even as delivery of computing services continues to explode. The shift to scale able and modular facilities has enabled substantial improvements in infrastructure efficiency evan as servers have become much more sophisticated in monitoring and controlling energy use.

This success is remarkable, but much more remains to be done. Most enterprise data centers operate at far lower efficiencies than their cloud computing counterparts, which makes them much more expensive to own and operate. Surprisingly, the solutions are now impeded primarily by management problems, not technology. Senior management routinely fails to understand the tight link between better energy performance and better business performance. Once that changes, the pace of efficiency improvements can proceed even more rapidly.

This talk will review these historical developments and describe how industry can do even better in coming years.

Dr. Jonathan G. Koomey is a researcher, author, lecturer, and entrepreneur whose work spans climate solutions, critical thinking skills, and the energy and environmental effects of information technology.

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